

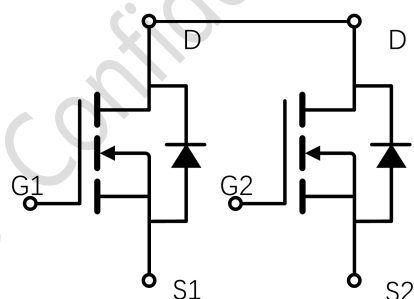
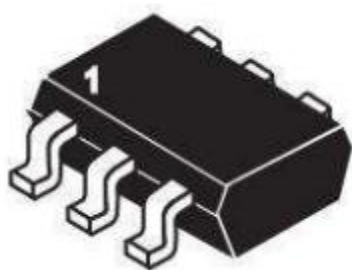
GENERAL DESCRIPTION

DP8205B uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

PRODUCT SUMMARY

VDS	20V
ID (at VGS=4.5V)	6.5A
RDS(ON) (at VGS = 4.5V)	<16mR
RDS(ON) (at VGS = 2.5V)	<21mR

TSSOP-8



ABSOLUTE MAXIMUM RATINGS $T_A=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	20	V
Gate-Source Voltage	VGS	± 12	V
Drain Current-Continuous @ $T_J=25^{\circ}\text{C}$	I_D	6.5	A
Pulsed ^b	I_{DM}	25	A
Drain-Source Diode Forward Current ^a	I_S	6.5	A
Maximum Power Dissipation ^a	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}\text{C}$

THERMAL CHARACTERISTIC

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient a	$R_{\theta JA}$	100	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typc	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=4,5A$	10	13.5	16	m Ω
		$V_{GS}=2.5V, I_D=3.5A$	12	16.5	21	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=4.5A$	-	10	-	S
Dynamic Characteristics						
Input Capacitance	C_{Iss}	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$	-	947	-	pF
Output Capacitance	C_{oss}		-	167	-	pF
Reverse Transfer Capacitance	C_{rss}		-	115	-	pF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A$ $V_{GS}=4.5V, R_{GEN}=6\Omega,$ $R_L=10\Omega$	-	10	20	nS
Turn-on Rise Time	t_r		-	11	25	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	70	nS
Turn-Off Fall Time	t_f		-	30	60	nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=6A,$ $V_{GS}=4.5V$	-	11	18	nC
Gate-Source Charge	Q_{gs}		-	3.2	-	nC
Gate-Drain Charge	Q_{gd}		-	1.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=1.7A$	-	0.79	1.2	V

Notes:

1. Surface Mounted on FR4 Board ,T<10 sec ;
2. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
3. Guaranteed by Design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

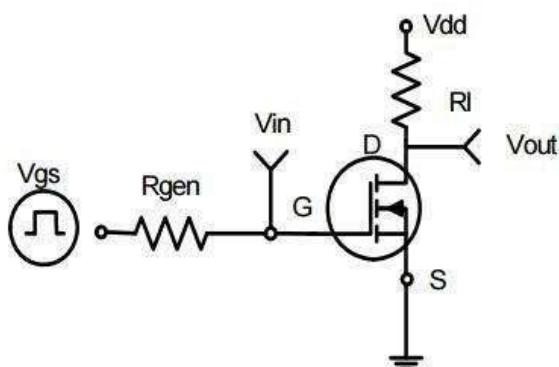


Figure 1: Switching Test Circuit

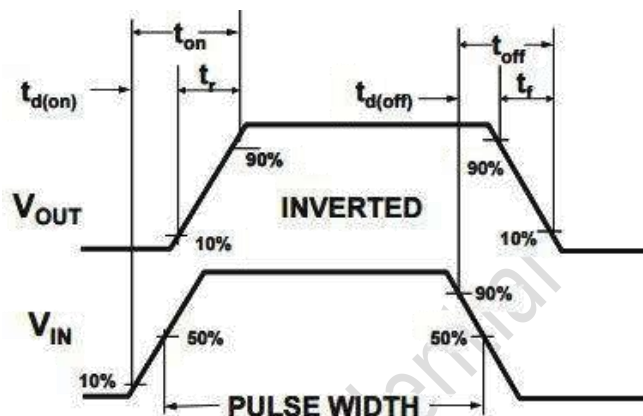


Figure 2: Switching Waveforms

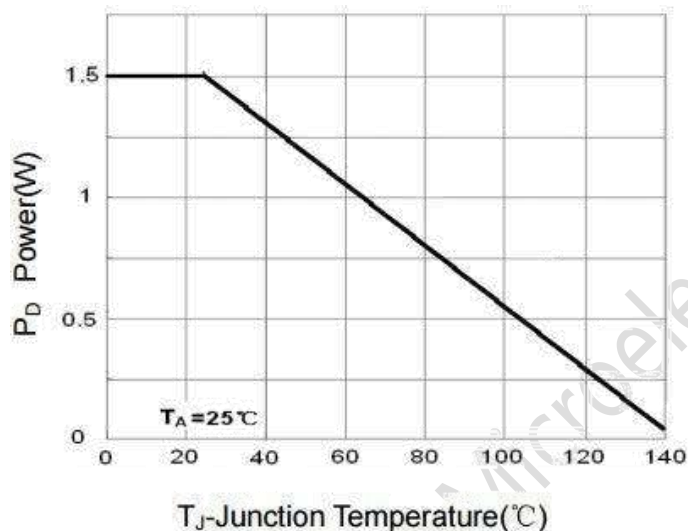


Figure 3: Power Dissipation

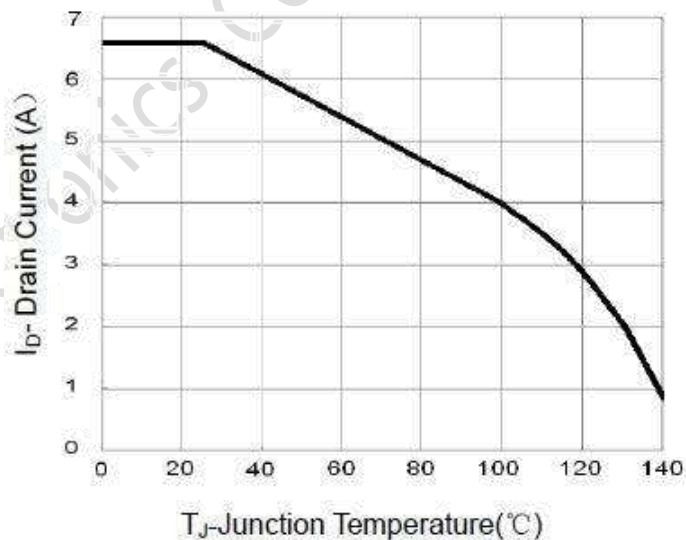


Figure 4: Drain Current

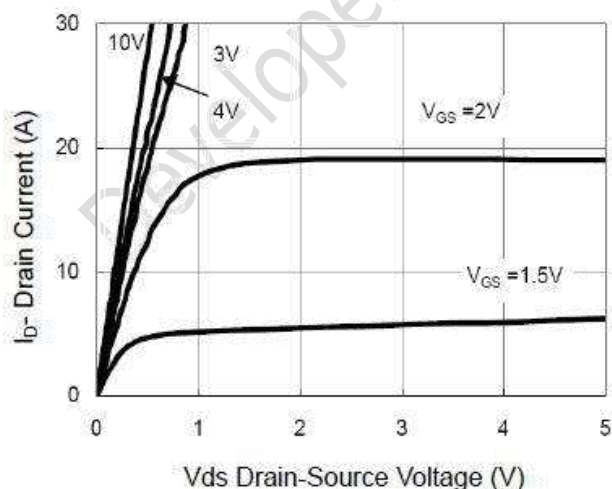


Figure 5: Output Characteristics

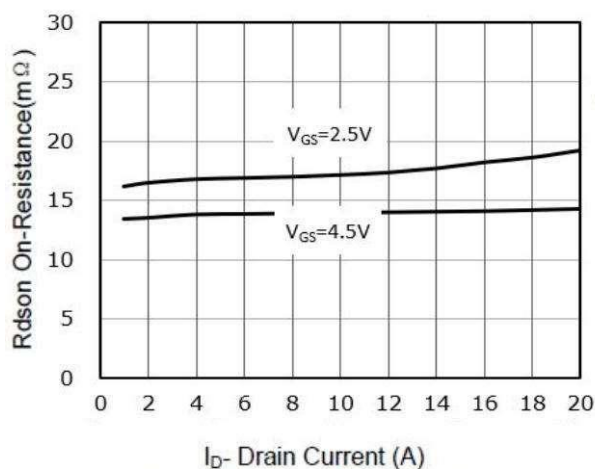


Figure 6: Drain-Source On-Resistance

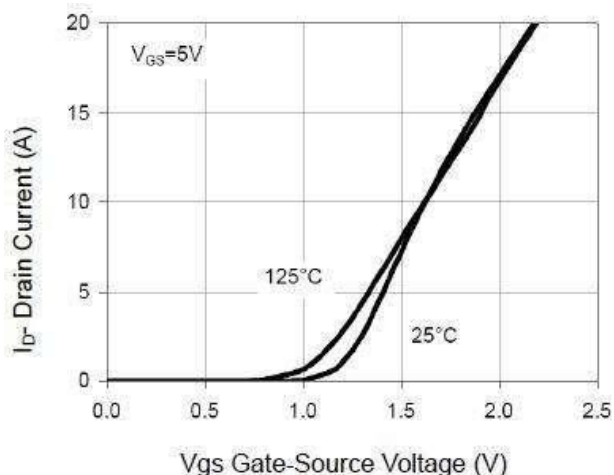


Figure 7 Transfer Characteristics

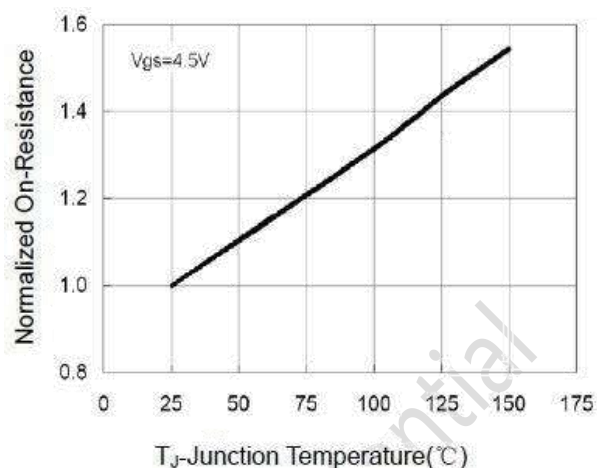


Figure 8 Drain-Source On-Resistance

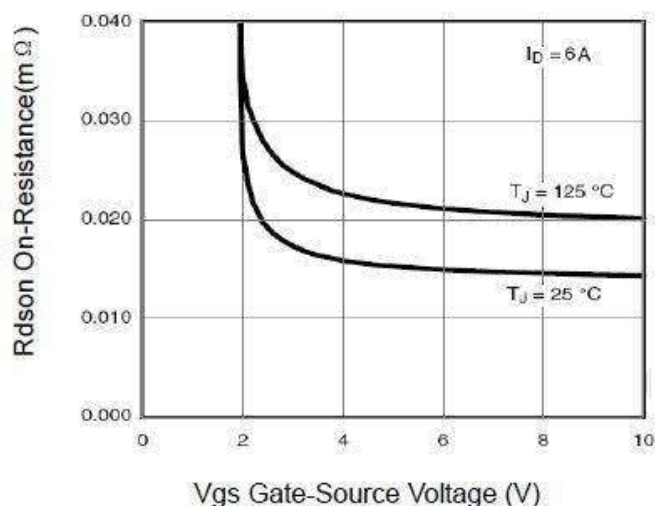


Figure 9 Rdson vs Vgs

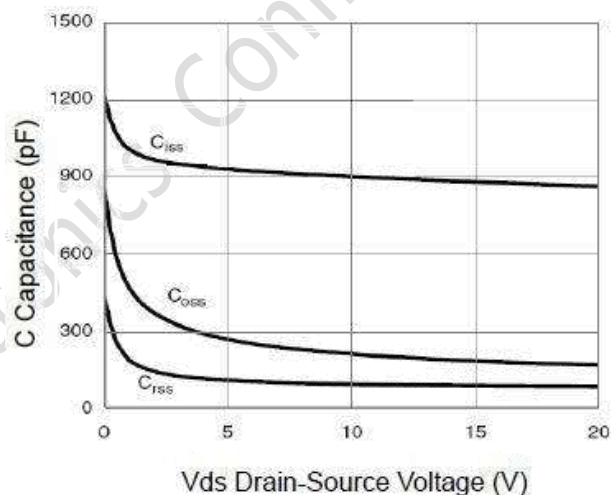


Figure 10 Capacitance vs Vds

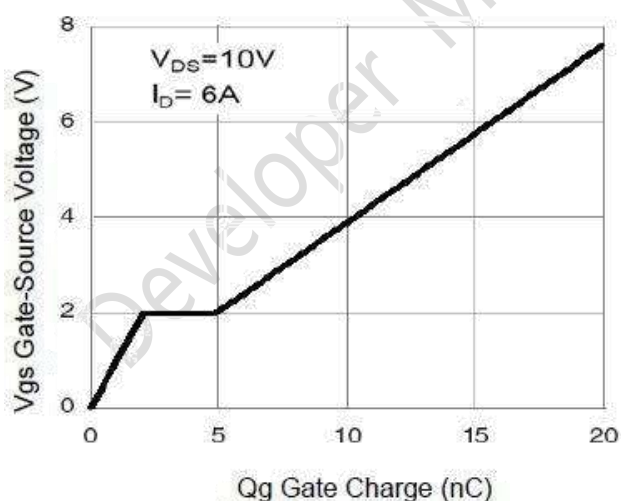


Figure 11 Gate Charge

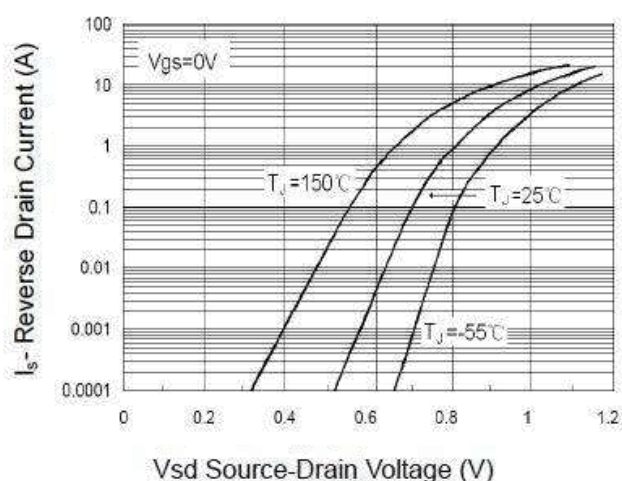


Figure 12 Source-Drain Diode Forward

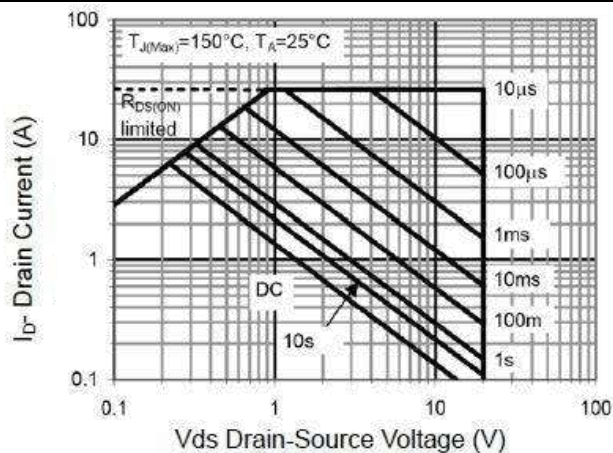


Figure 13 Safe Operation Area

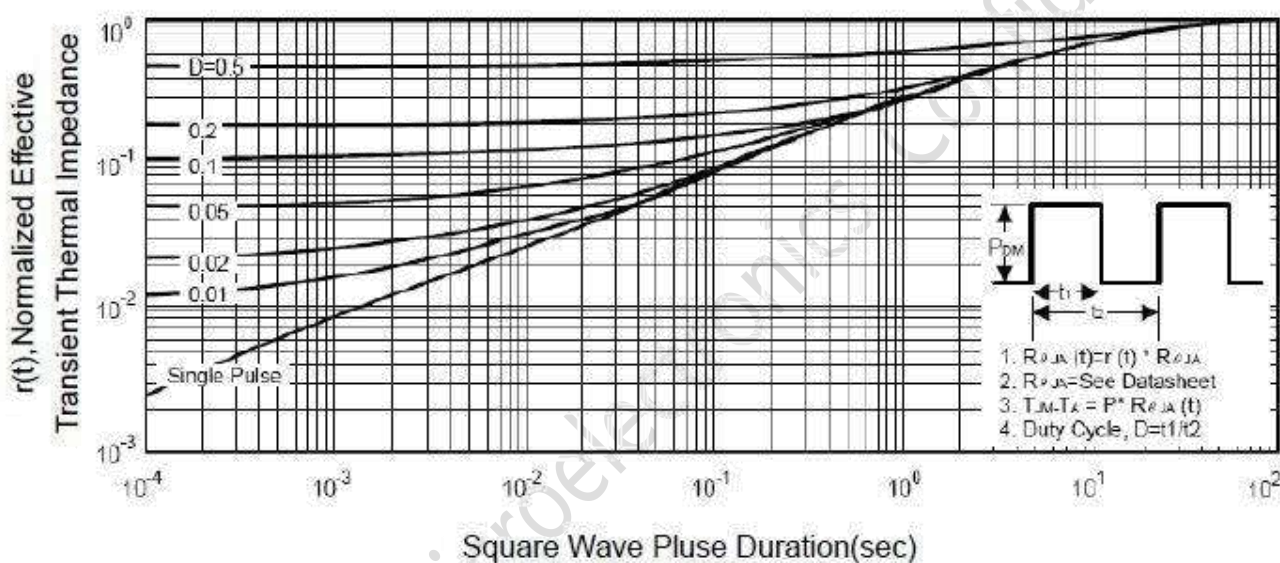
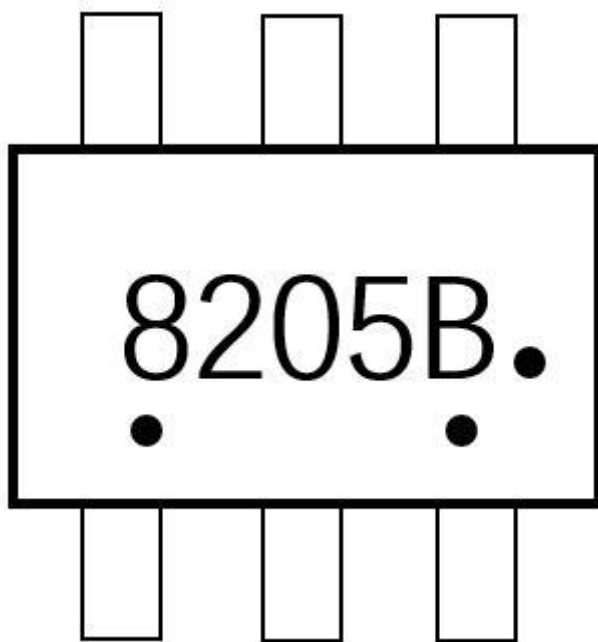


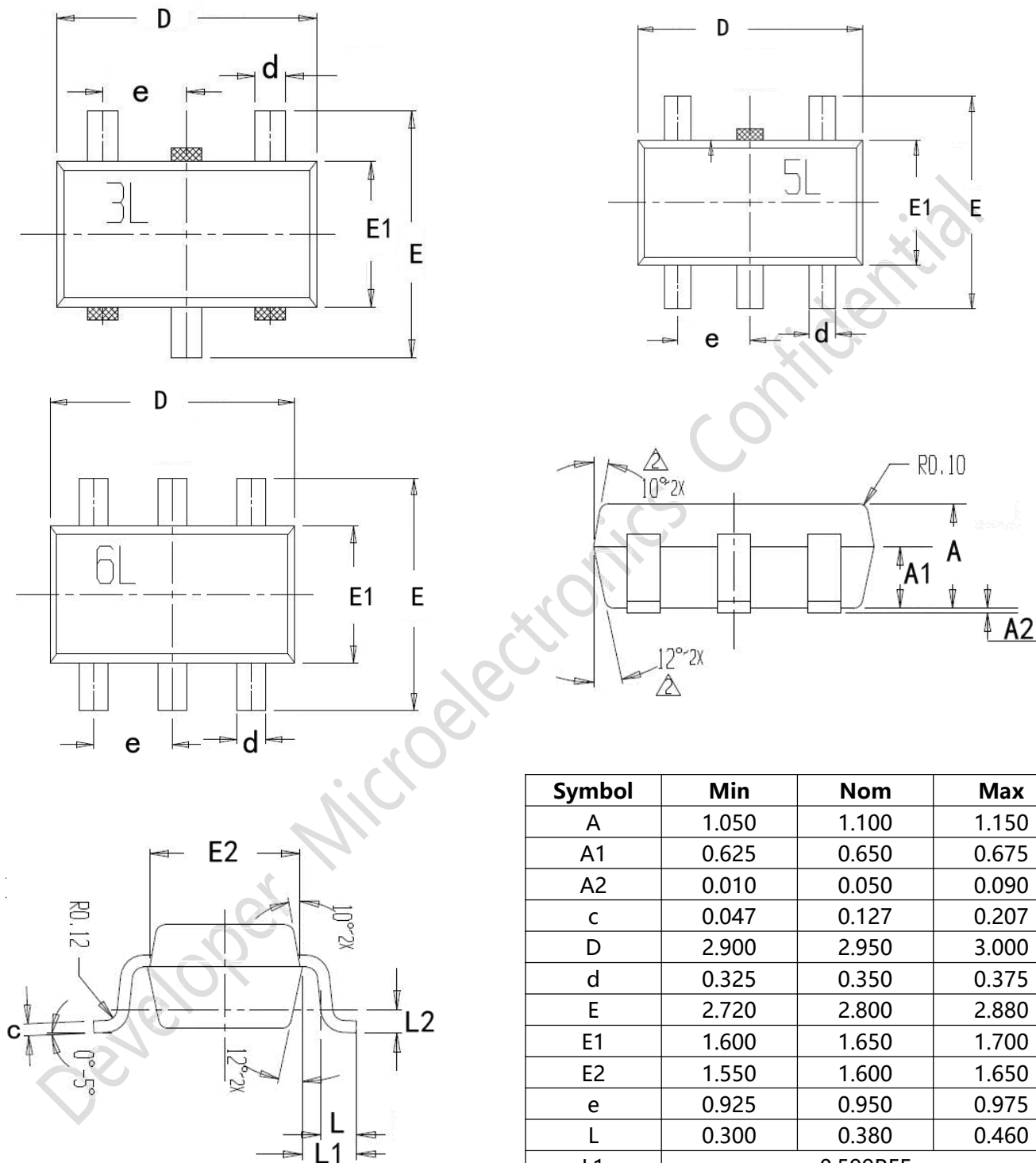
Figure 14 Normalized Maximum Transient Thermal Impedance



MARKING DESCRIPTION

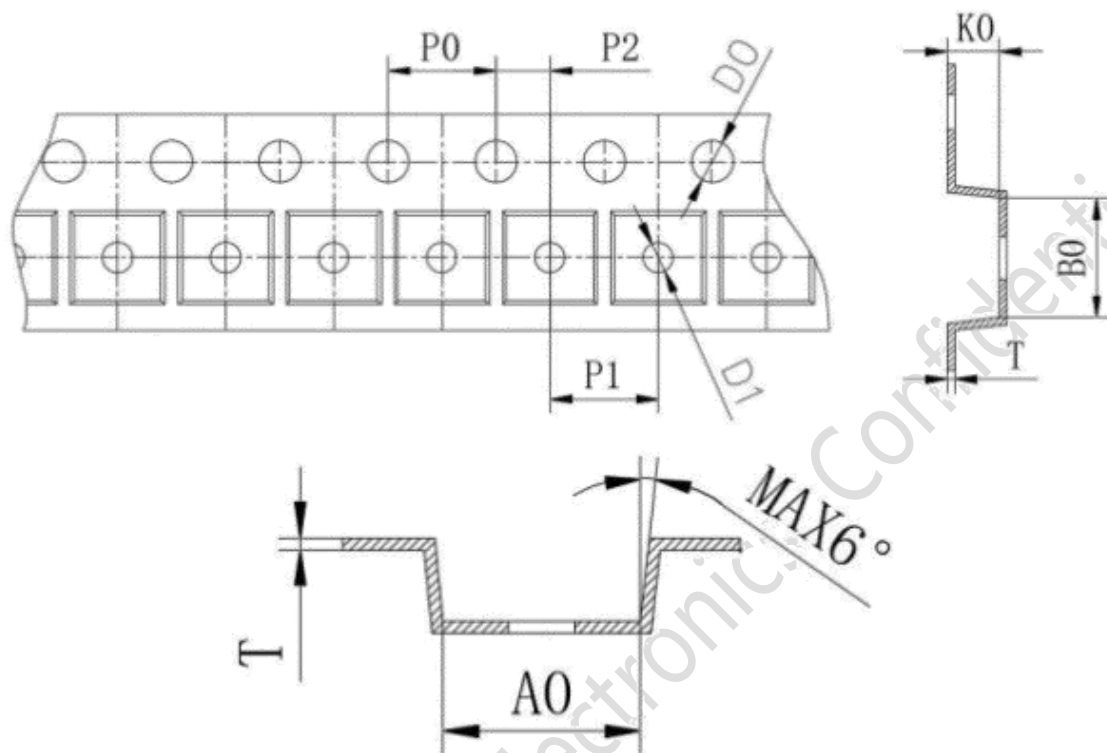


PACKAGE OUTLINE DIMENSIONS



TAPE SIZE

SOT23-6



SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	3.23 ± 0.10	3.17 ± 0.10	1.37 ± 0.10	4.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.20 ± 0.05	1.75 ± 0.10	3.50 ± 0.05	1.55 ± 0.05	1.10 ± 0.10	$8.00^{+0.20}_{-0.10}$

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