LED display control drive IC

1 Overview

DP32129 is a serial decoding common cathode driver chip specially designed for LED scanning screen.It integrates 8-channel NMOS Row switch circuit, supports arbitrary scanning, and has the functions of high-performance shadow elimination self-adaptation, led lamp bead short circuit and LED lamp opening circuit string light processing.DP32129 can completely replace the original 3-8 decoder (74HC138) circuit of LED module, more effectively simplify the complexity of LED module PCB wiring, thereby improving the overall image effect of the display screen.

2 Features

- Working voltage 3.5V~5.5V
- Supports arbitrary scanning
- Integrate 8-channel NMOS
  - OUT_MAX = 2.5A @ VDD = 5.0V
  - RON=90mΩ@VDD=5.0V&IOUT=1.0A
- Max power consumption < 600 MW @ VDD = 5.0V
- Integrate shadow elimination self-adaptation function, effectively eliminating Row shadow
- Configure the blanking voltage through the register to adapt more complex environments
- Improve LED cross-hair phenomenon of display caused by LED lamp open circuit
- Simplify the complexity of LED module PCB wiring
- Encapsulation：SOP16
- High ESD level

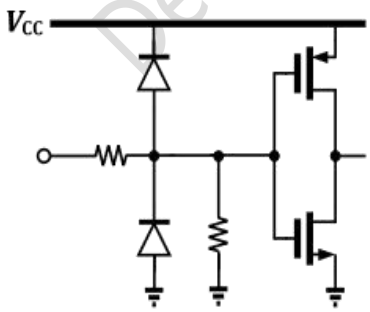
3 Application field

- High refresh rate LED video display
- Full- color LED display
- High-density and small-spacing LED panel display

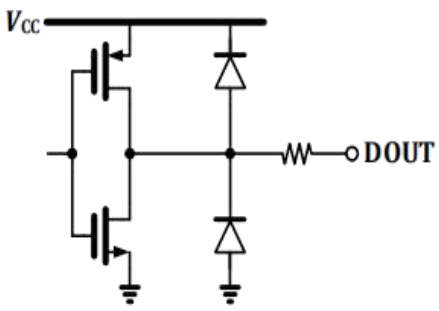
4 Circuit schematic diagram

4.1 Input and Output Equivalent Circuit

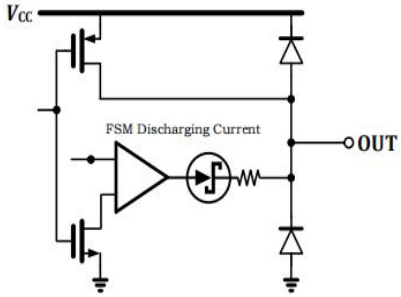
SDI,LATCH,SCK Input terminals



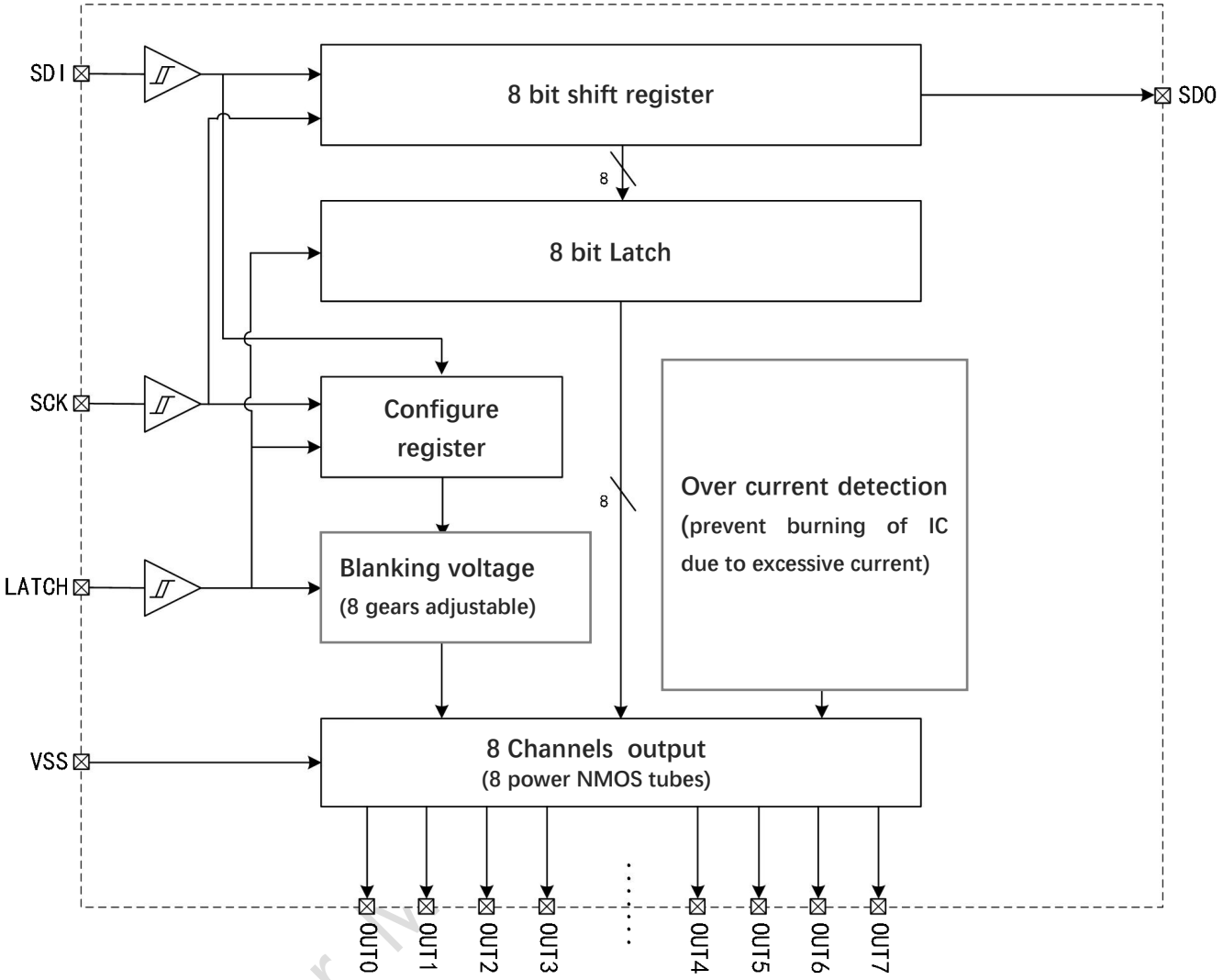
DOUT Output



OUT0~7 Output terminals



4.2 Internal Circuit Block Diagram



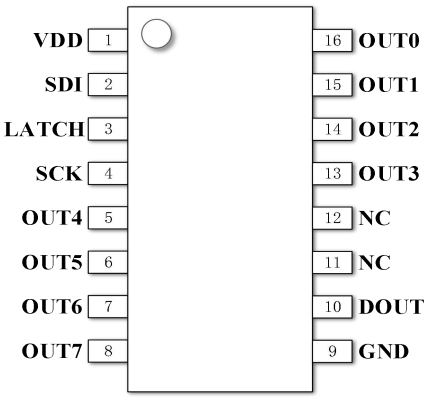
Contents

Revision History

Version	Date modified	Reviser	Revised contents
V1.0	2023.08	WM	1.Initial Version
V1.1	2024.03	LXZ	1.Fix pin naming of application block diagram
V1.2	2024.06	WM	1.Fix Timing constraints 2.Fix default value of blanking voltage
V1.3	2025.03	WM	1. Fix Row switch Control

5 Product Description

- PIN Definition



SOP16 Pin definition diagram

- PIN Description

SOP16 PIN No.	PIN Name	PIN Description
1	VDD	Power input
2	SDI	Data input
3	LATCH	Data latch signal
4	SCK	Data clock signal
5~8，13~16	OUT0~OUT7	Output
9	GND	Power ground
10	DOUT	Serial Data Output
11，12	NC	Empty PIN

- Package Information

Product Name	Encapsulation style	Packing style	Quantity/ tray	Moisture sensitivity grade
DP32129	SOP16	Tape packaging	4000	MSL=3

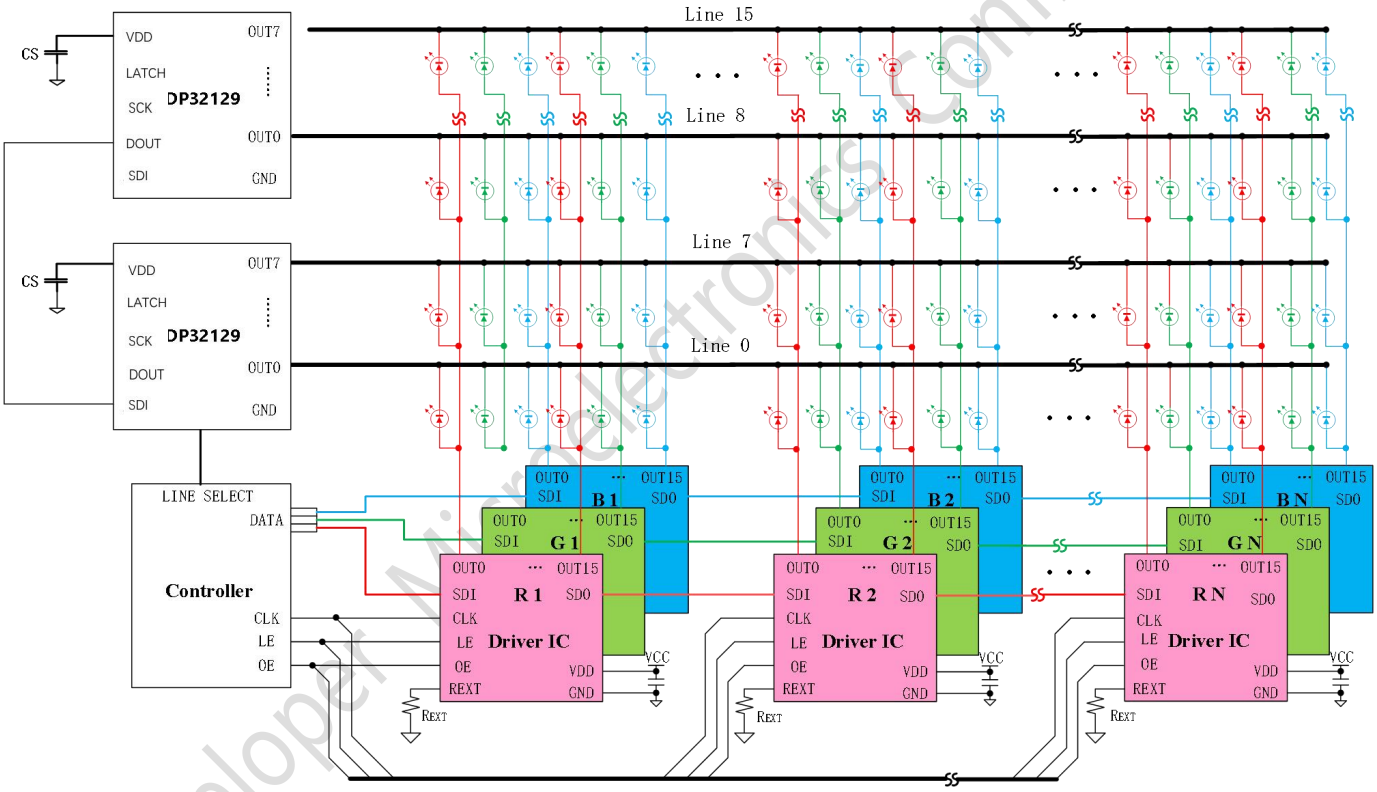
- Product marking

SOP16

DP32129 is the product Name;
XXXXXX represents the product batch number ;

6 Proposed Application Circuit

The LED scanning screen is widely used in indoor display screen to reduce the cost, but the parasitic capacitance of the LED anode will instantaneously generate a discharge path when scanning, resulting in the smear phenomenon of the display screen;The user can use the DP32129 with the discharge circuit function and refer to the recommended application circuit of the scanning screen as shown in the figure below, and use the constant current driver chip DP3269S with the built-in pre-charging function, so that the upper and lower smears can be completely eliminated.Because DP32129 is an 8-channel output integrated power chip, in order to avoid excessive heat accumulation, it is recommended to use the display screen with more than 16 scans, and pay attention to the temperature condition when using.



LED display 16 Scans application block diagram

7 Parameter list

7.1 Maximum limit parameter

Project	Symbol	Rated value	Unit
Power supply voltage	V_{CC}	0~6.0	V
Input Voltage	V_{IN}	-0.4~V_{DD}+0.4	V
Continuous working output current	I_D	-2.5	A
Instantaneous maximum output current	I_{OUT_MAX}	-3.5	A
Power Loss	PD	<600	mW
Package thermal resistance	$R_{th(j-a)}$	80	℃/W
Operating temperature	T_{opr}	-40~85	℃
Storage Temperature	T_{stg}	-40~150	℃
Human body model (HBM)	V_{ESD}	≥8	KV

- All the voltage value setting based on Chip ground port (GND) as reference, the test temperature of the maximum limit parameter is 25℃;
- Application exceed the above specified value, may cause permanent damage to components, extending the operating life under absolute maximum conditions may reduce the reliability of the components. These are only part of the specified values, and do not support the functional operation of other conditions beyond the specification;
- SMD components, soldering peak temperature must be lower than 260℃, temperature curve as standard J-STD-020, and factory decides by itself, take the reference by actual situation and solder paste manufacture’ s suggestion;

7.2 Recommended Work Scope

Project	Symbols	Conditions	Min value	Standard value	Max value	Unit
Power supply voltage	V_{CC}	-	3.5	5.0	5.5	V
Output terminal voltage (DOUT)	V_{DOUT}	-	0.7	-	V_{DD}	V
Output terminal current (DOUT)	I_{OH}	V_{OH} =V_{DD} -0.5V	-	-16	-	mA
	I_{OL}	V_{OL} =0.5V	-	20	-	
Input voltage (SDI,LATCH,SCK)	V_{IH}	V_{DD}=3.3V~5.5V	0.7 V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	

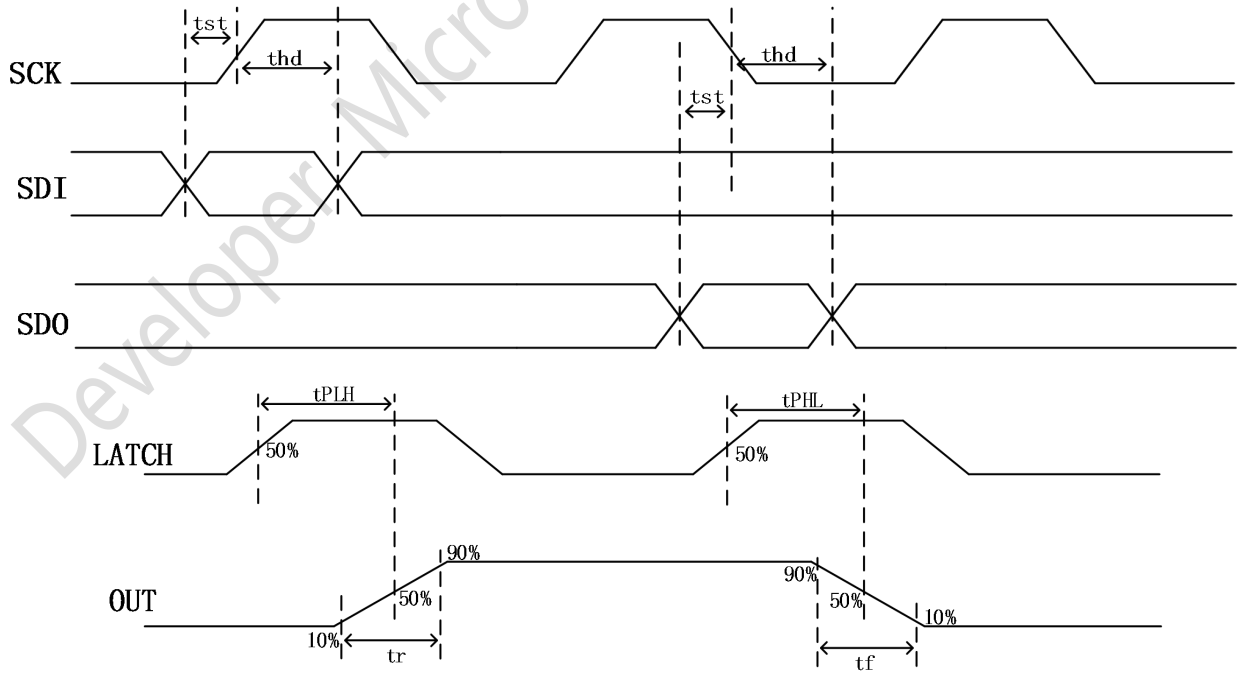
7.3 DC Electrical Characteristics (VDD=5.0V)

Project		Symbols	Conditions	Min value	Standard value	Max value	Unit
Logic power supply voltage		V_{DD}	-	3.0	5.0	5.5	V
Power terminal current		I_{DD_OFF}	All output are set low	-	400	-	uA
Gate opening voltage		$V_{GS(th)}$	V_{DS}=VGS,I_D=250uA	-	-0.7	-0.9	V
Source-drain pole conduction resistance		$R_{DS(on)[1:7]}$	V_{GS}=-5.0V, I_{OUT}=-1.0A	-	90	-	mΩ
Input voltage	High level	V_{IH}	logic level voltage	0.7 V_{DD}	-	V_{DD}	V
	Low level	V_{IL}		0	-	0.3 V_{DD}	

7.4 Dynamic Property (Without special instructions, VDD=3.5V~5V, Ta=25℃)

Project	Symbols	Test conditions	Min value	Standard value	Max value	Unit
Output rise delay	t_{PLH}	VDD=5.0V CL=12pF	-	50	-	ns
Output drop delay	t_{pHL}		-	100	-	ns
Output rising edge	t_r		-	60	-	ns
Output drop edge	t_f		-	400	-	ns
Setup time	t_{st}		60	-	-	ns
Hold time	t_{hd}		60	-	-	ns

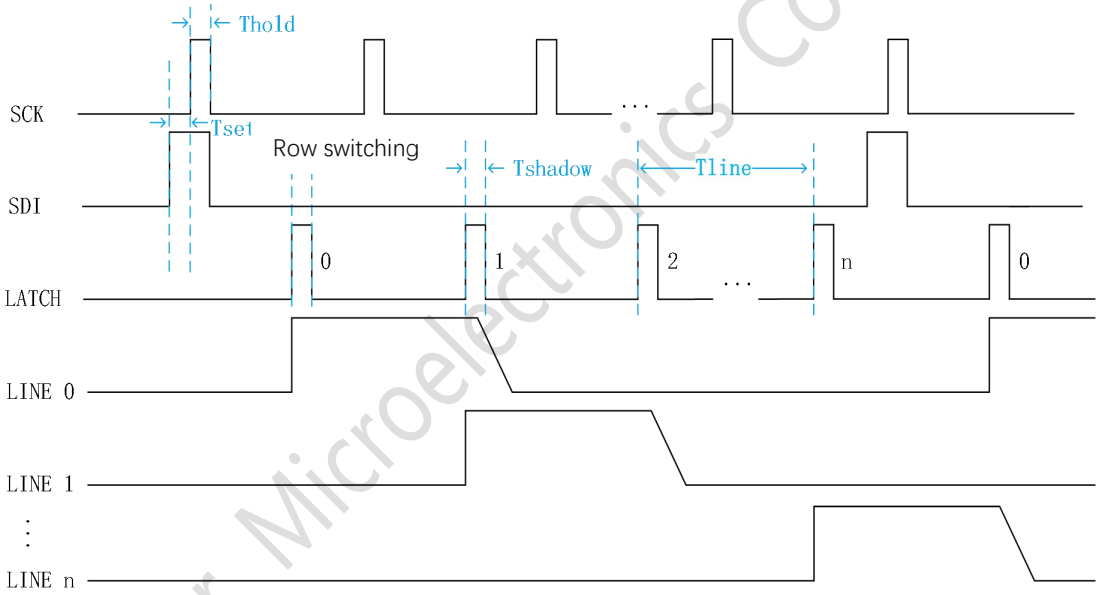
8 Timing waveform



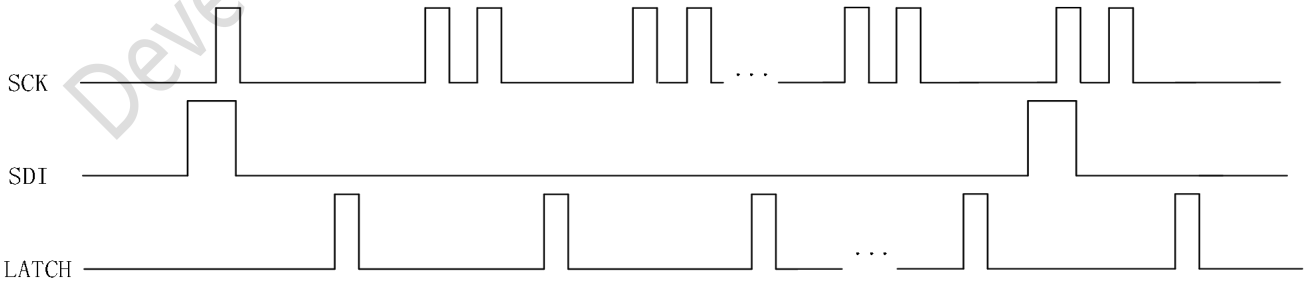
9 Row switch Control and blanking Time

DP32129 is a common cathode display serial decoder line tube driver, where each Row Switch is fixed to send 1 LATCH, and the channel output is high effective; the input data SDI to the output data DOUT is fixed to be at the rising edge interval of 8 SCK.

Symbols	Description	Min value	Max value
Tshadow	Equal to LATCH signal high level width	500ns	-
Tsetup	Setup time	60ns	-
Thold	Hold time	60ns	-



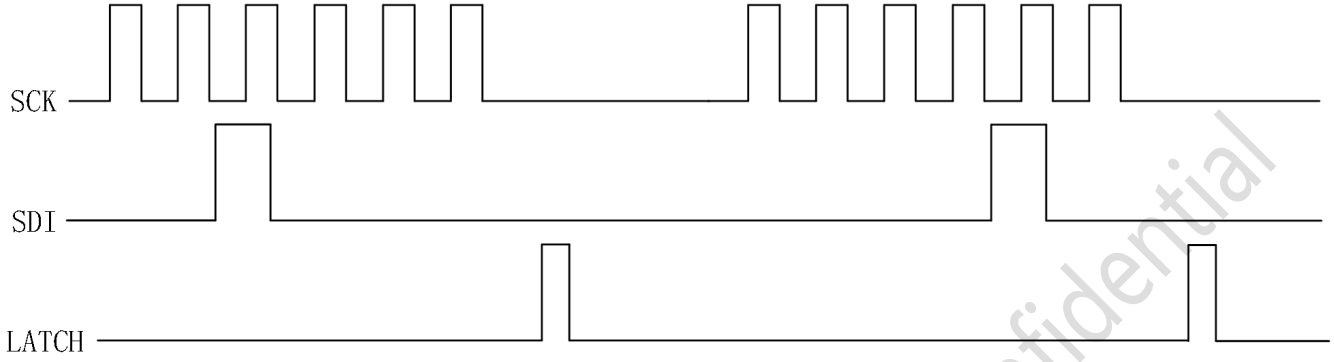
Scan the waveform line by line



Interlaced scanning configuration waveform

Number of rows =6 as an example:

Send 6 SCK impulses，only one SCK rising edge samples to SDI high level，others SCK rising edge is sampled to SDI low level，The time from the back to the front is recorded as the first, the second..6th SCK rising edge.If the NTH SCK rising edge is sampled to the SDI high level, Step 2 enable the display of the NTH channel.



Configure waveform for any scan

10 Configure register

DP32129 Built in 4bit register:

BIT	Name	Default	Description		
3	VR_UP[2]	1′ b1	Pull up the erasing circuit reference potential configuration register ,the highest bit in VR_UP[2:0]		
2	reserved	1′ b0	reserved		
1:0	VR_UP[1:0]	2′ b10	Pull up the cancellation circuit reference potential according to the register, VR_UP[2:0] can be set to (Vdd=5V)-		
			0000：Vdd*7/20 =1.75V 0001：Vdd*8/20 =2.0V 0010：Vdd*9/20 =2.25V 0011：Vdd*10/20 =2.5V	1000 ： Vdd*11/20 =2.75V 1001 ： Vdd*12/20 =3.0V 1010：Vdd*13/20 =3.25V 1011 ： Vdd*15/20 =3.5V	Default 2.75V **Data pin matching：** SDI corresponds to c signal of 3-8 decoding; LATCH corresponds to A signal of 3-8 decoding ; SCK corresponds to B signal of 3-8 decoding;

Symbol	Description	Minimum value	Maximum value
Tsetup1	Setup time	60ns	-
Thold1	Hold time	60ns	-

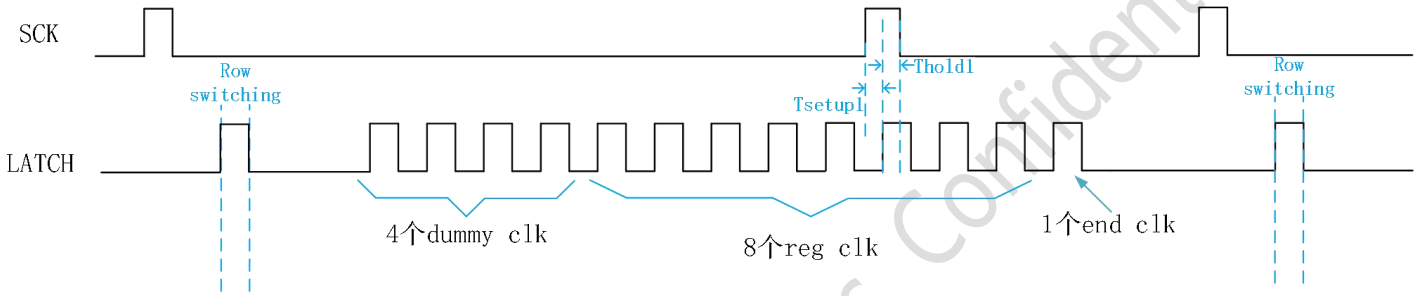
Configuration Register mode:

Register configuration is completed by two signals, SCK and LATCH, the configuration waveform is divided into three steps as shown below:

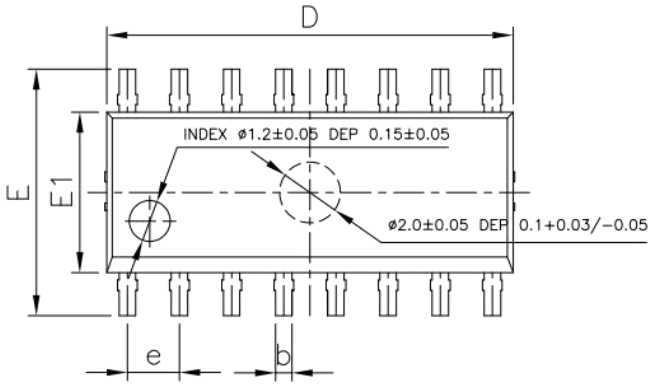
(1)LATCH sends four dummy CLK pulses, and the chip enters register configuration after receiving them.

(2)LATCH continues to send 8 CLK pulses, and the value of the sampled SCK of the NTH LATCH pulse is stored in the NTH bit of the register (N=1~8).

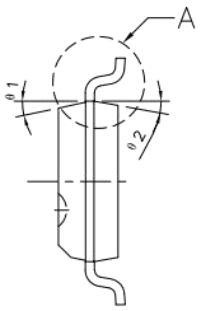
(3)LATCH continues to send one CLK pulse, which the chip receives and exits the register configuration state.



11 Package Dimensions



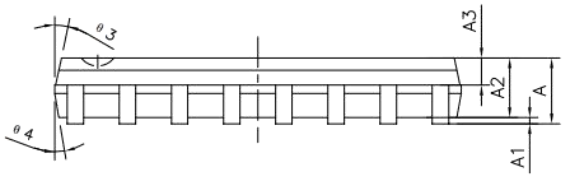
TOP VIEW



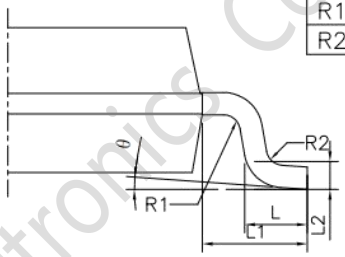
SIDE VIEW

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX
A	–	–	1.70
A1	0.10	0.15	0.20
A2	1.42	1.45	1.48
A3	0.62	0.65	0.68
b	0.38	–	0.51
D	9.85	9.90	9.95
E	5.90	6.00	6.10
E1	3.87	3.90	3.93
e	1.24	1.27	1.30
L	0.50	0.60	0.70
L1	1.05REF		
L2	0.25REF		
θ	0°	–	8°
θ1-θ4	12°REF		
R1	0.15REF		
R2	0.15REF		



SIDE VIEW



DETAIL A

12 Official Announcement

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