DP8810

Dual N-Channel Enhancement Power MOSFET

GENERAL DESCRIPTION

DP8810 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. It is ESD protected. This device is suitable for use as a Battery protection or in other Switching application.

PRODUCT SUMMARY

V_{DS}	20 V
I_D (at V_{GS}=4.5V)	6.0A
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 20mΩ
$R_{DS(ON)}$ (at V_{GS} = 2.5V)	< 25mΩ
ESD Rating: 2000V HBM	

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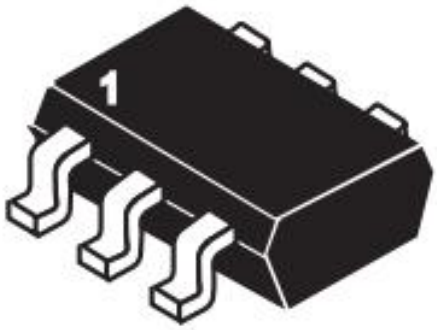

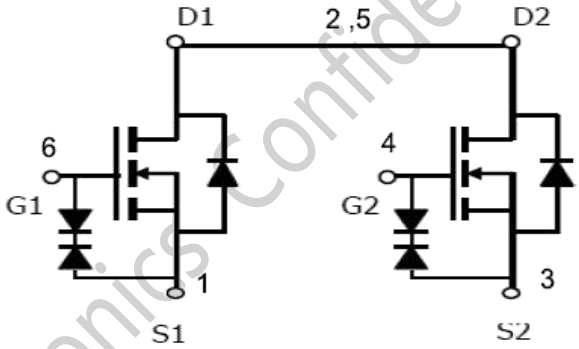

ABSOLUTE MAXIMUM RATINGS (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±8	V
Drain Current-Continuous @ T_J=25℃	I_D	6	A
Pulsed[b]	I_{DM}	30	A
Maximum Power Dissipation[a]	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

THERMAL CHARACTERISTIC

Parameter	Symbol	Limit	Unit
Thermal Resistance,Junction-to-Ambient [a]	$R_{\theta JA}$	83.3	℃/W

ELECTRICAL CHARACTERISTICS (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Off Characteristics						
Drain-Source Breakdown	BV_{DSS}	V_{GS}=0V I_D=250μA	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=16V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±8V,V_{DS}=0V	-	-	±10	μA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.55	0.7	1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=6A	-	14	20	mΩ
		V_{GS}=2.5V, I_D=5A	-	17	25	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=6A	-	20	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=10V, V_{GS}=0V, F=1.0MHz	-	650	-	pF
Output Capacitance	C_{oss}		-	140	-	pF
Reverse Transfer Capacitance	C_{rss}		-	60	-	pF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V, I_D=1A, V_{GS}=5V, R_{GEN}=3Ω ,	-	0.5	-	nS
Turn-on Rise Time	t_r		-	1	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	12	-	nS
Turn-Off Fall Time	t_f		-	4	-	nS
Total Gate Charge	Q_g	V_{DS}=10V, I_D=6A, V_{GS}=4.5V	-	8	-	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	nC
Gate-Drain Charge	Q_{gd}		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=1.7A	-	-	1.2	V
Drain-Sourse Diode Forward	I_S	V_{GS}=0V	-	-	2.0	A

Notes:

a. Surface Mounted on FR4 Board ,T<10 sec ;

b. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

c. Guaranteed by Design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

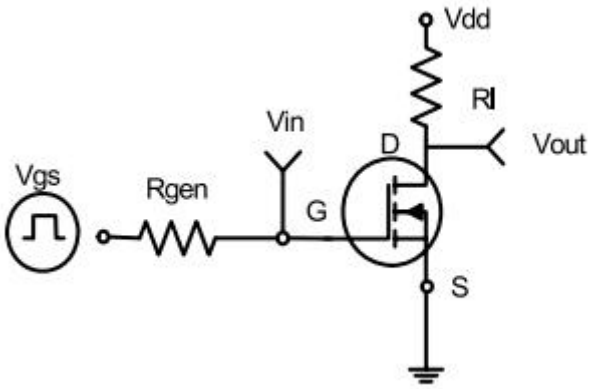

Figure 1: Switching Test Circuit

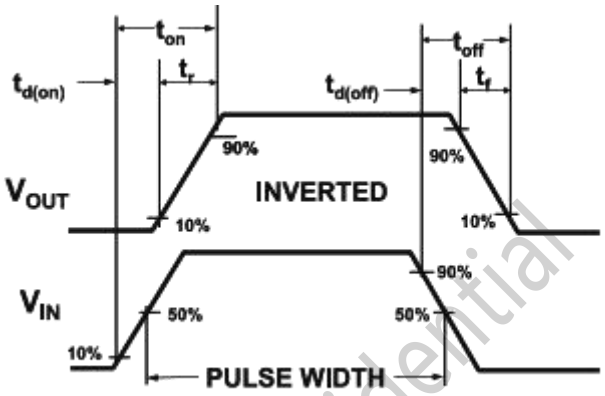

Figure 2: Switching Waveforms

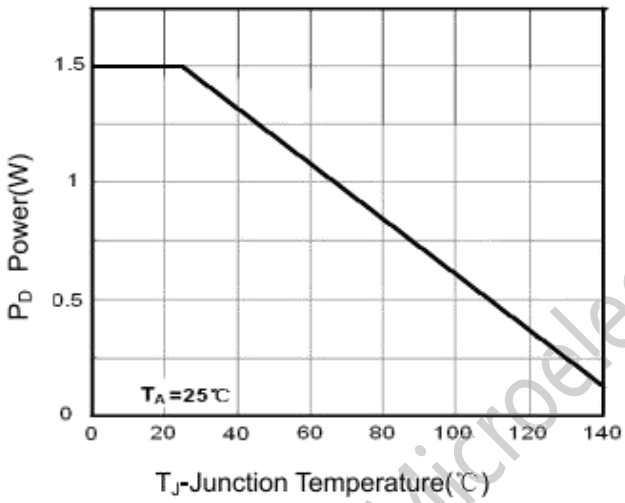

Figure 3: Power Dissipation

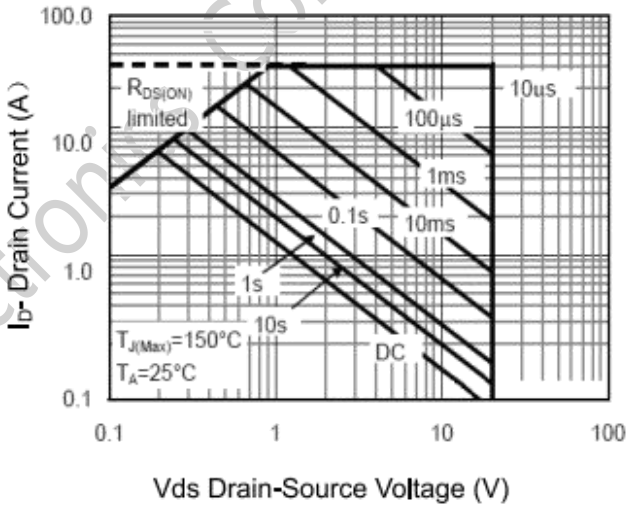

Figure 4: Safe Operation Area

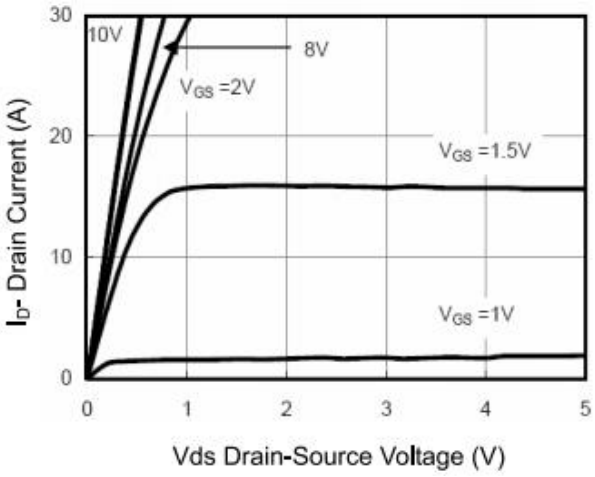

Figure 5: Output Characteristics

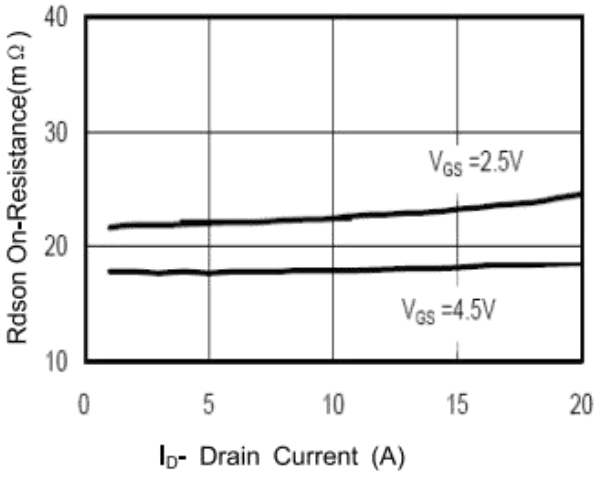

Figure 6: Drain-Source On-Rsistance

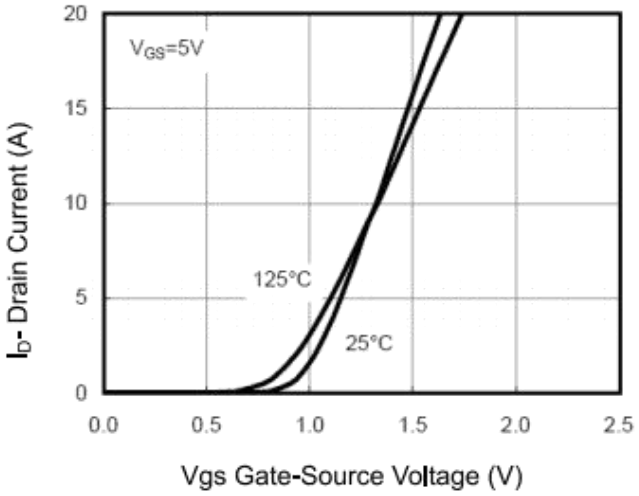

Figure 7: Transfer Characteristics

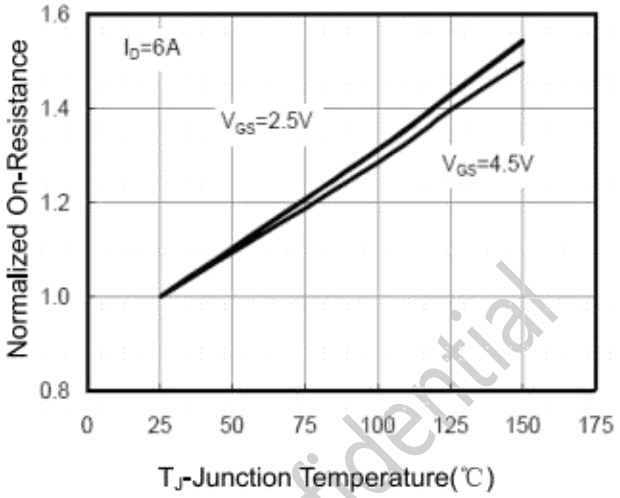

Figure 8: Drain-Source On-Rsistance

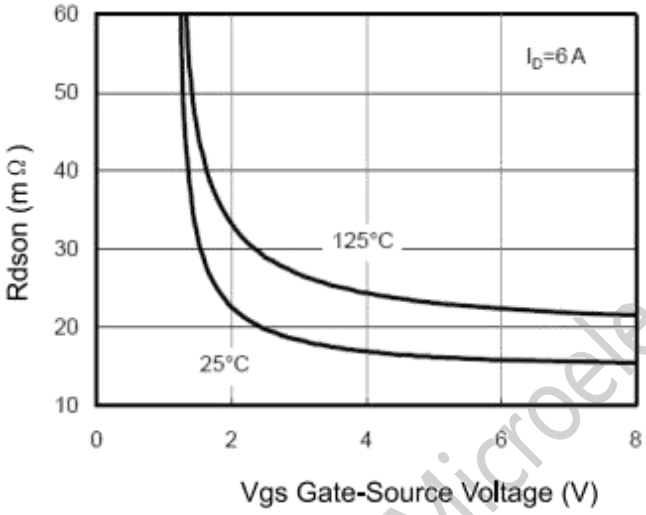

Figure 9: $R_{DS(ON)}$ VS V_{GS}

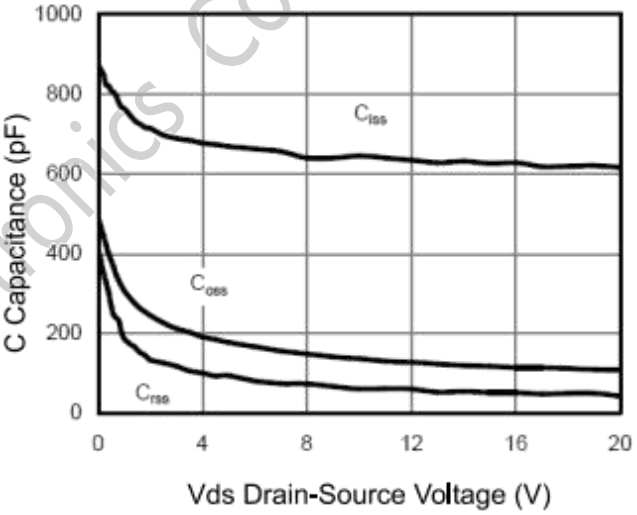

Figure 10: Capacitance VS V_{DS}

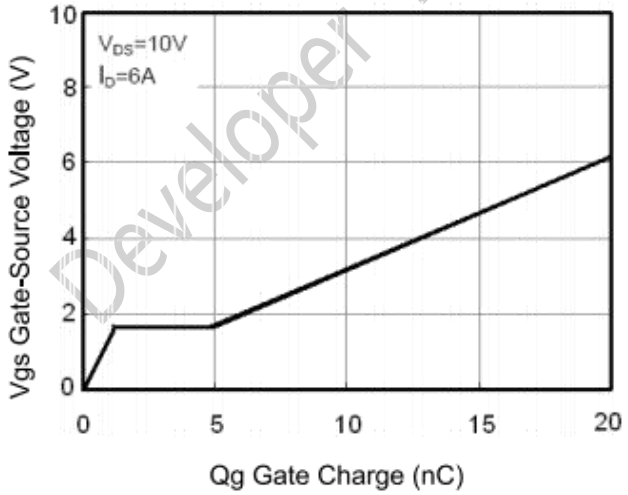

Figure 11: Gate Charge

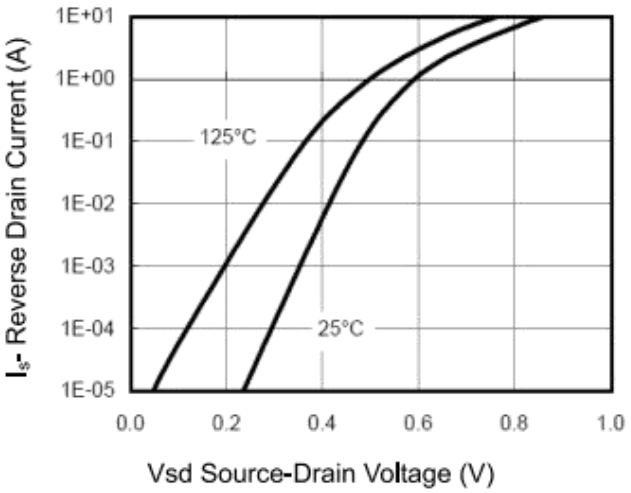

Figure 12: Source-Drain Diode Forward

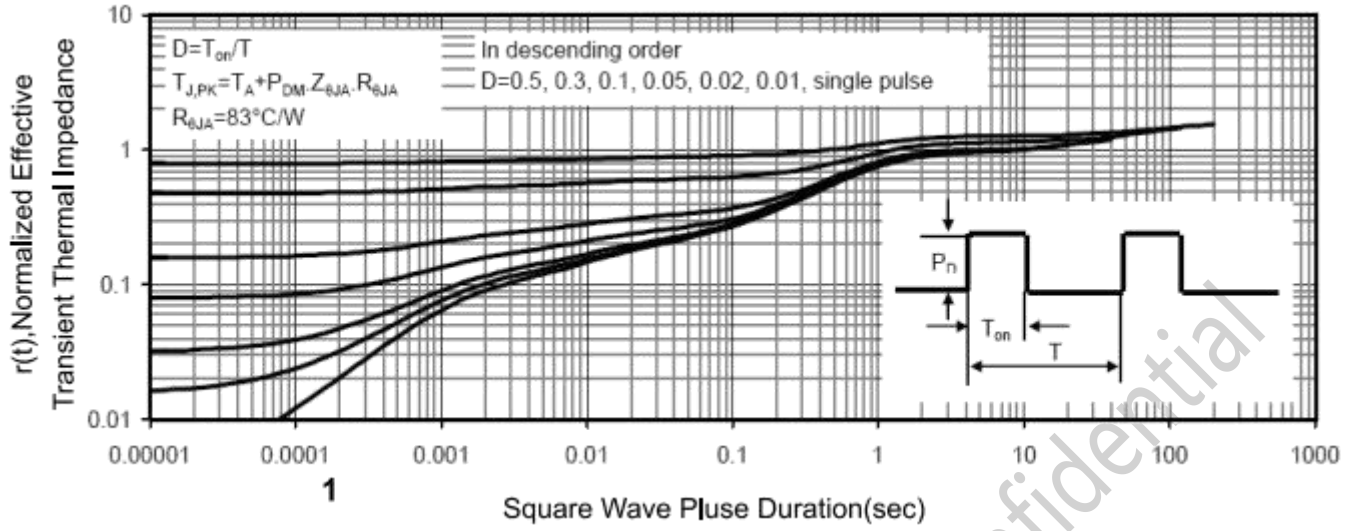

Figure 13: Normalized Maximum Transient Thermal Impedence

MARKING DESCRIPSION

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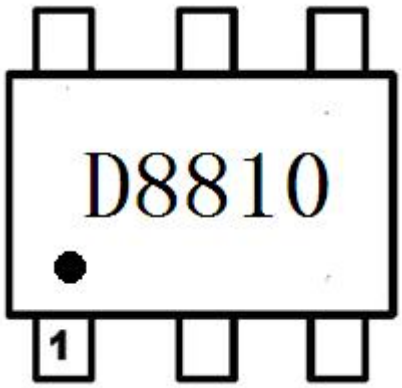

PACKAGE OUTLINE DIMENSIONS

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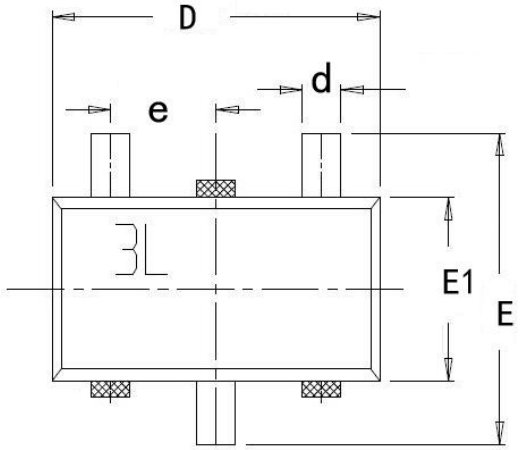

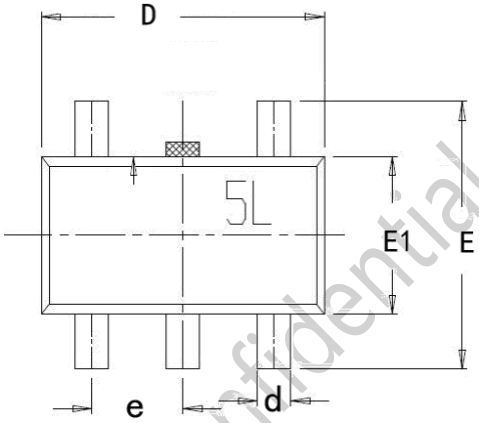

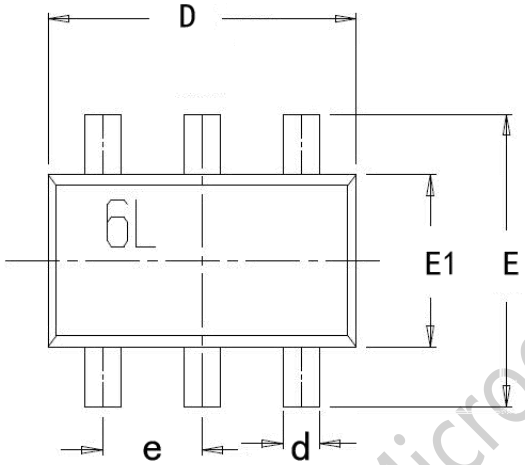

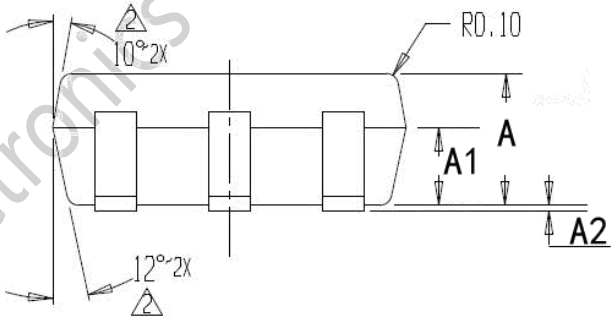

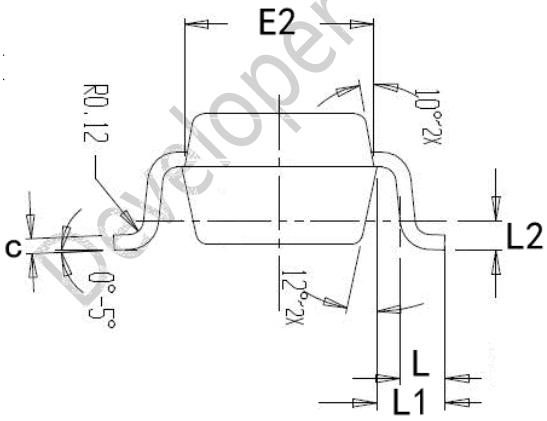

Symbol	Min	Nom	Max
A	1.050	1.100	1.150
A1	0.625	0.650	0.675
A2	0.010	0.050	0.090
c	0.047	0.127	0.207
D	2.900	2.950	3.000
d	0.325	0.350	0.375
E	2.720	2.800	2.880
E1	1.600	1.650	1.700
E2	1.550	1.600	1.650
e	0.925	0.950	0.975
L	0.300	0.380	0.460
L1	0.599REF		
L2	0.250BSC		

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