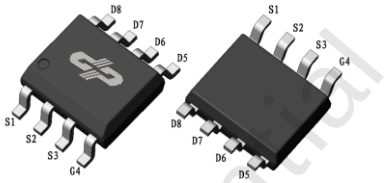
DP200N02STL

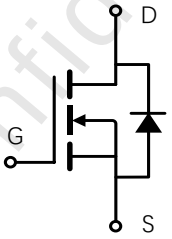
TRMOS N-MOSFET 20V, 12.5mΩ, 13A

Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$ (@V_{GS}=4.5V)	$R_{DS(on).typ}$ (@V_{GS}=2.5V)	I_D
DP200N02STL	20V	12.5mΩ	15.5mΩ	13A

SOP-8





100% Avalanche Tested

100% Rg Tested

Features

- Advanced high cell density Trench MOSFET technology
- Better $R_{DS(on)}$ enabled by a low $R_{DSon.sp}$, low conduction losses
- Excellent Q_gx$R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

Applications

- Battery management
- Power Management Switches

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP200N02STL	200N02STL	SOP-8	Reel

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	20	V
Continuous drain current T_A = 25°C T_A = 100°C	I_D	 13 8	A
Pulsed drain current (T_A= 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	52	A
Avalanche energy, single pulse (I=0.5mH, Rg=25)[1]	E_{AS}	40	mJ
Gate-Source voltage	V_{GS}	±12	V
Power dissipation (T_A = 25°C)	P_{tot}	5	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C

[1].EAS is tested at starting T_j = 25℃, V_{GS} = 4.5V.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, Junction-to-Lead	R_{thJL}	25	°C/W

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	20	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	0.4	0.7	1	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=20V,V_{GS}=0V T_j=25°C
		-	-	100		T_j=85°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±12V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	12.5	17	mΩ	T_j=25°C V_{GS}=4.5V, I_D=15A
		-	15.5	21	mΩ	V_{GS}=2.5V, I_D=10A
Gate resistance	R_g	-	1.5	5	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz
Transconductance[2]	g_{fs}	-	70	-	S	V_{DS}=5V,I_D=8A
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	752	-	pF	V_{GS}=0V, V_{DS}=10V, f=1MHz
Output Capacitance	C_{oss}	-	154	-		
Reverse Transfer Capacitance	C_{rss}	-	89	-		
Gate Total Charge(V_{GS}=10V)	Q_g	-	9	-	nC	V_{GS}=10V, V_{DS}=10V, I_D=10A, f=1MHz
Gate Total Charge(V_{GS}=4.5V)	Q_g	-	4	-		
Gate-Source charge	Q_{gs}	-	2.5	-		
Gate-Drain charge	Q_{gd}	-	1.7	-		
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	V_{GS}=4.5V, V_{DD}=10V, R_{G_ext}=2.7Ω
Rise time	t_r	-	3.5	-		
Turn-off delay time	$t_{d(off)}$	-	20	-		
Fall time	t_f	-	6	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0V,I_{SD}=10A
Diode continuous forward current	I_s	-	13	-	A	T_A = 25°C
Diode pluse current	$I_{s\ pluse}$	-	52	-	A	T_A = 25°C
Body Diode Reverse Recovery Time[2]	t_{rr}	-	25	-	ns	I_F=10A, dI/dt=300A/μs
Body Diode Reverse Recovery Charge[2]	Q_{rr}	-	14	-	nC	

[2]. Defined by design. Not subject to production test

Typical Performance Characteristics

Fig 1: Output Characteristics

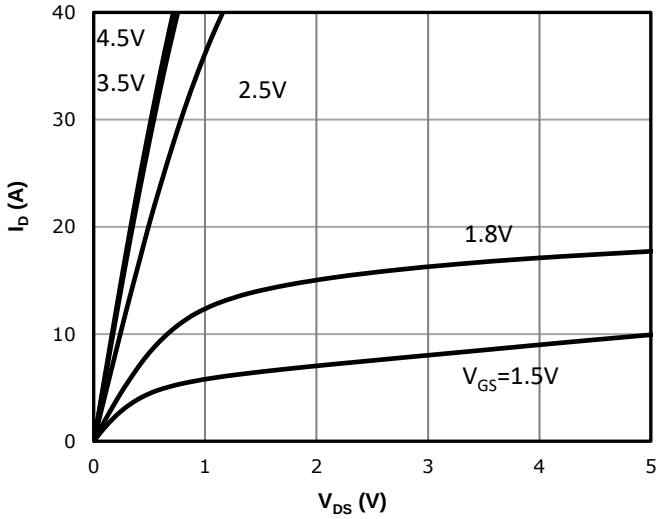


Fig 2: Transfer Characteristics

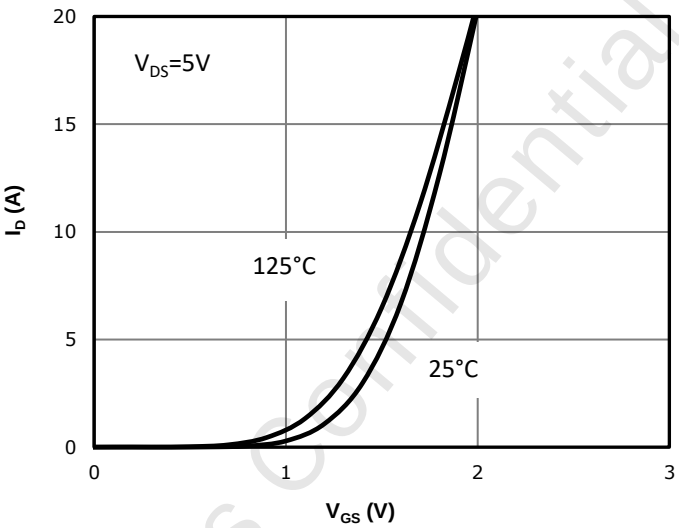


Fig 3: Rds(on) vs Drain Current and Gate Voltage

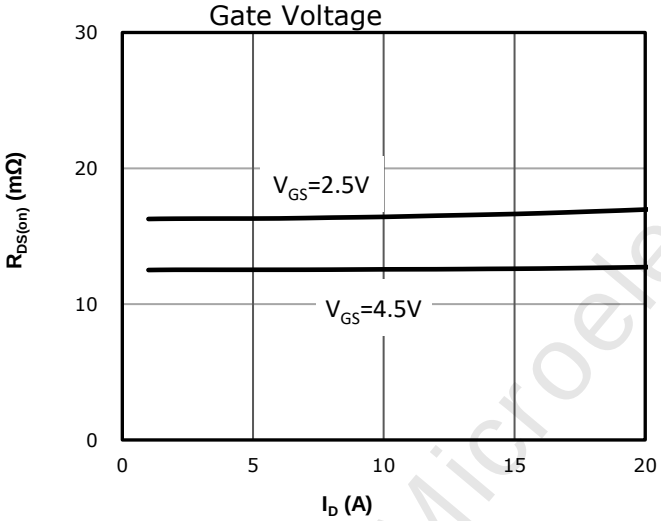


Fig 4: Rds(on) vs Gate Voltage

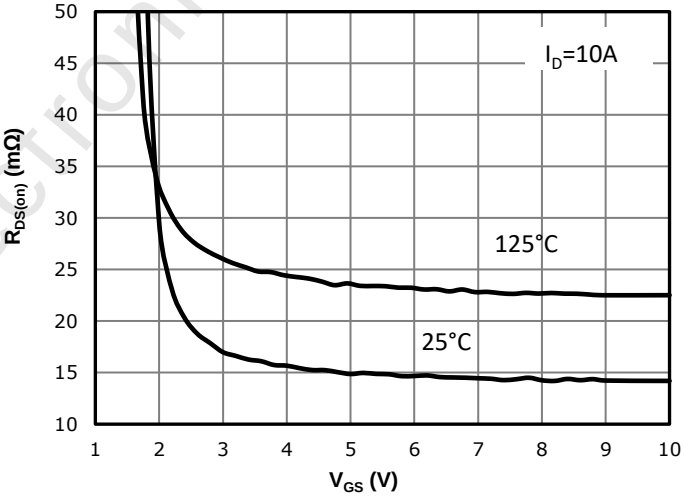


Fig 5: Rds(on) vs. Temperature

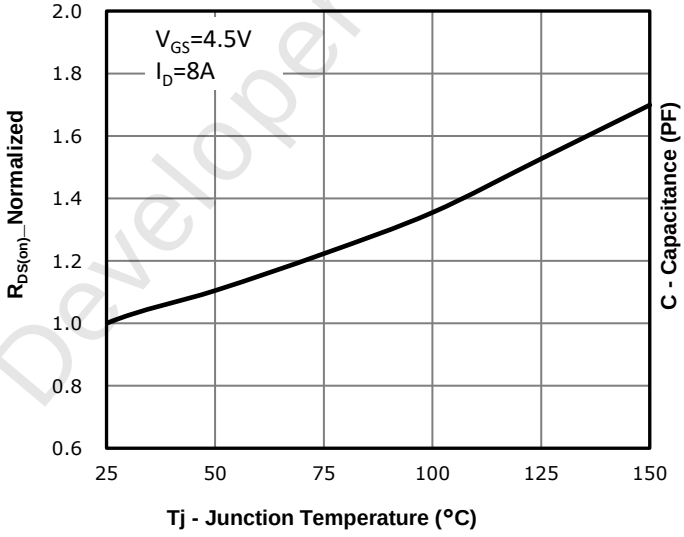


Fig 6: Capacitance Characteristics

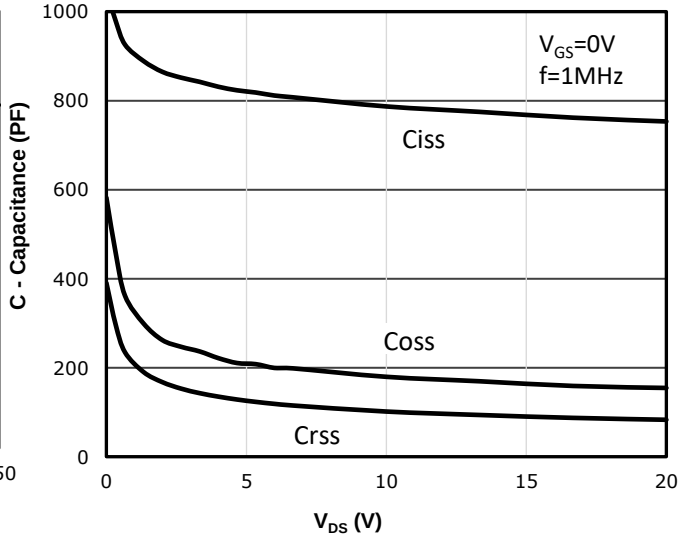


Fig 7: Gate Charge Characteristics

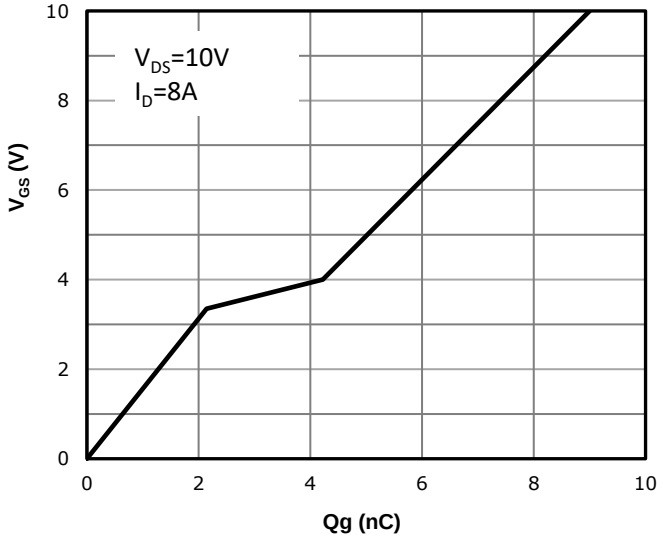


Fig 8: Body-diode Forward Characteristics

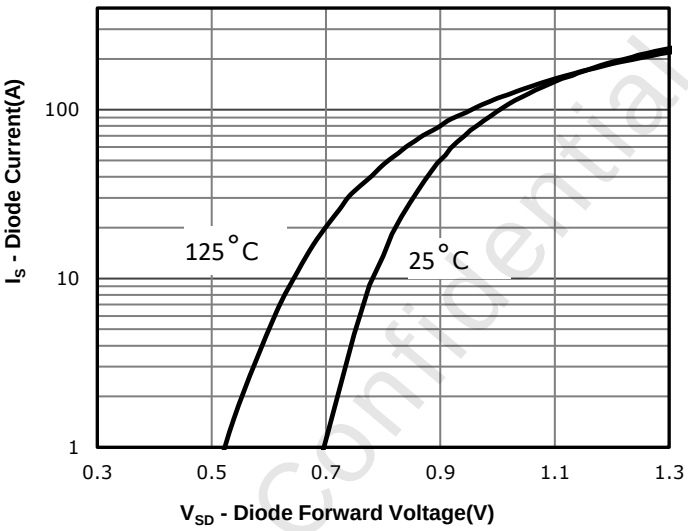


Fig 9: Power Dissipation

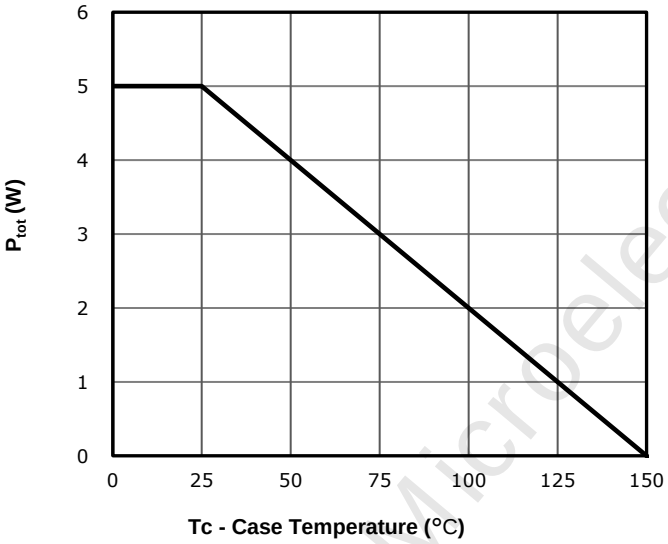


Fig 10: Drain Current Derating

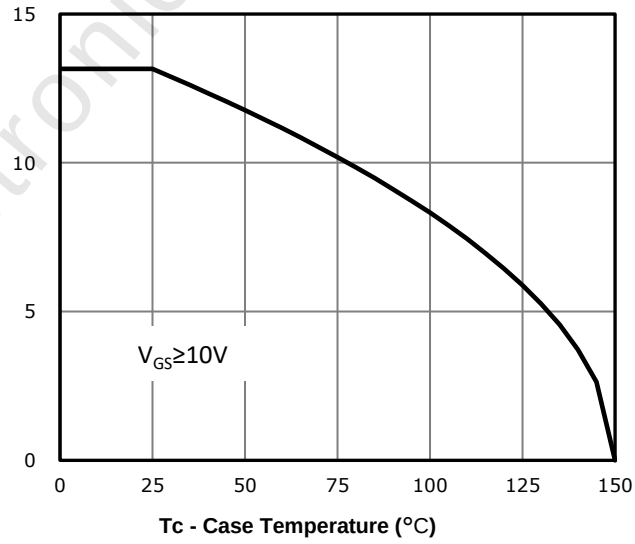


Fig 11: Safe Operating Area

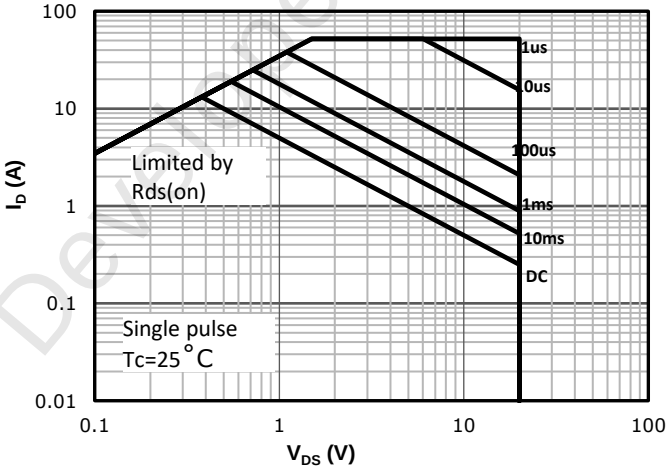
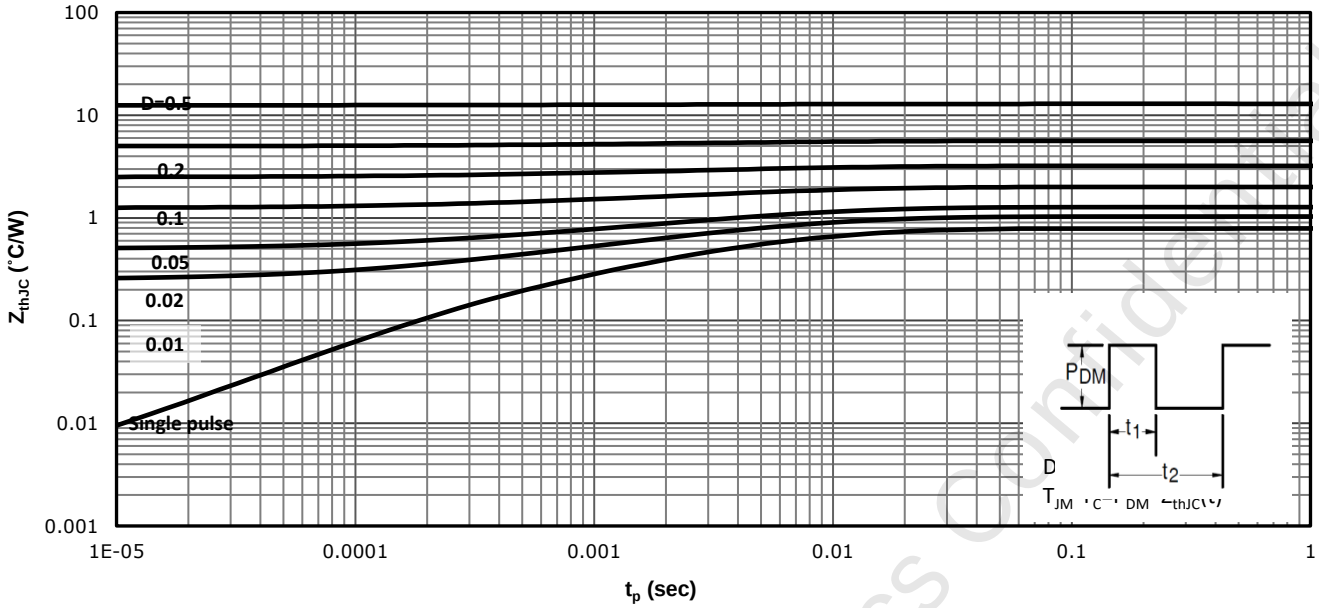
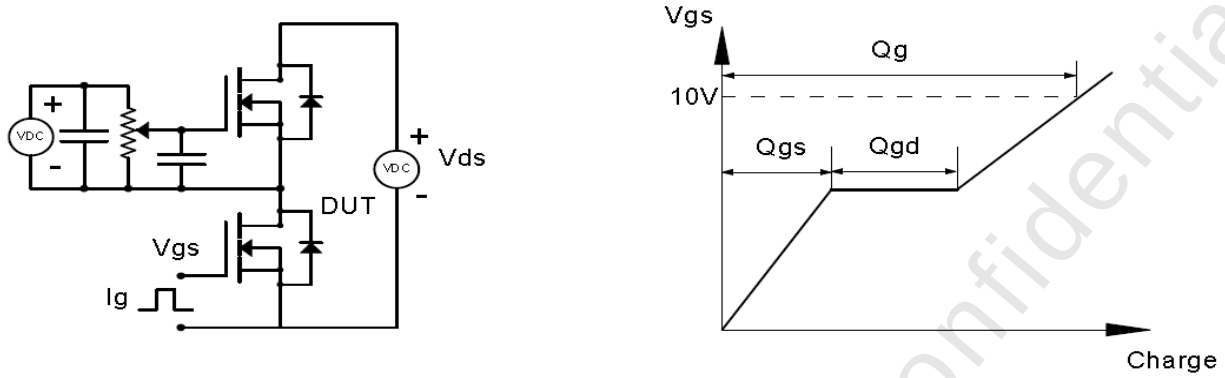


Fig 12: Max. Transient Thermal Impedance

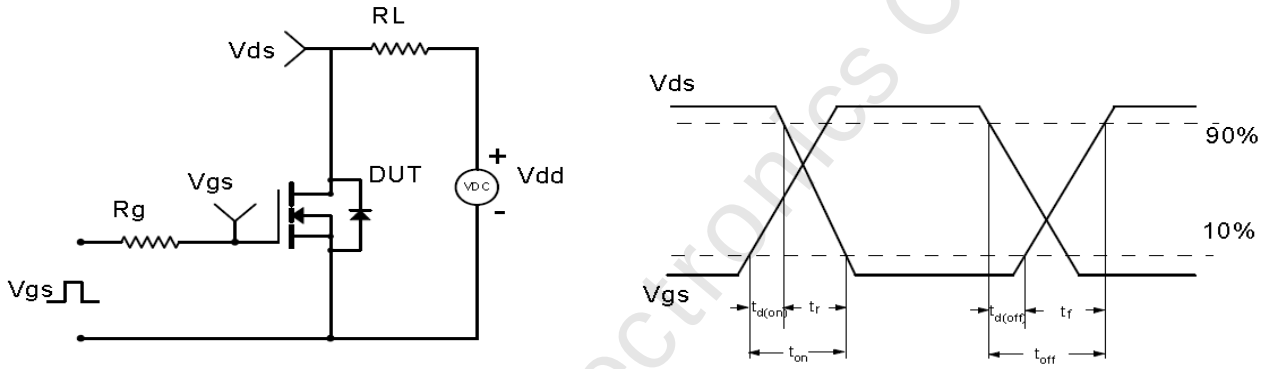


Test Circuit & Waveform

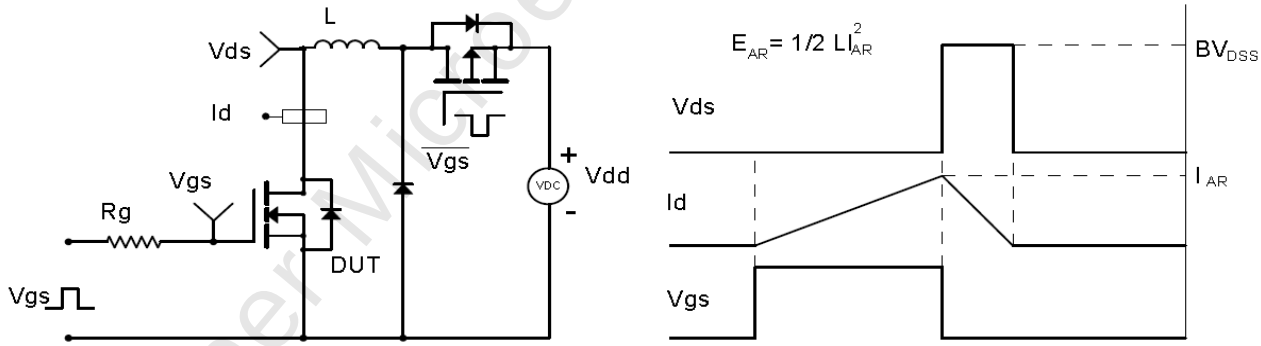
Gate Charge Test Circuit & Waveform



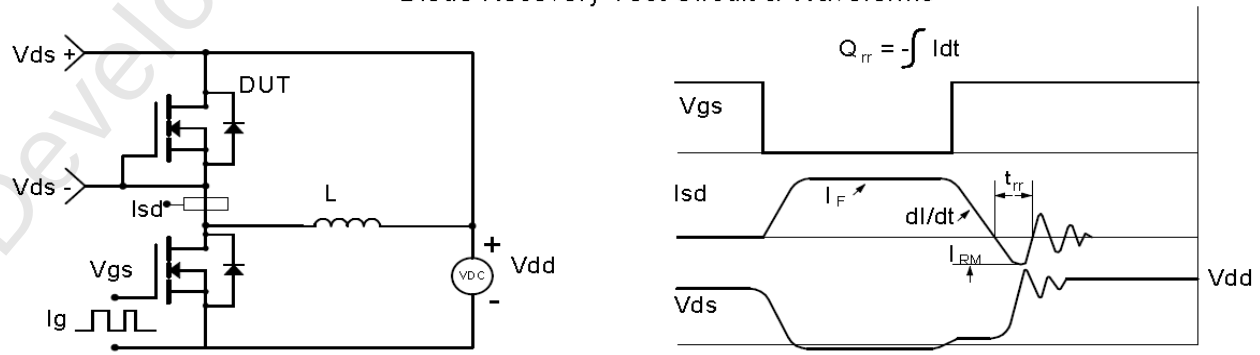
Resistive Switching Test Circuit & Waveforms



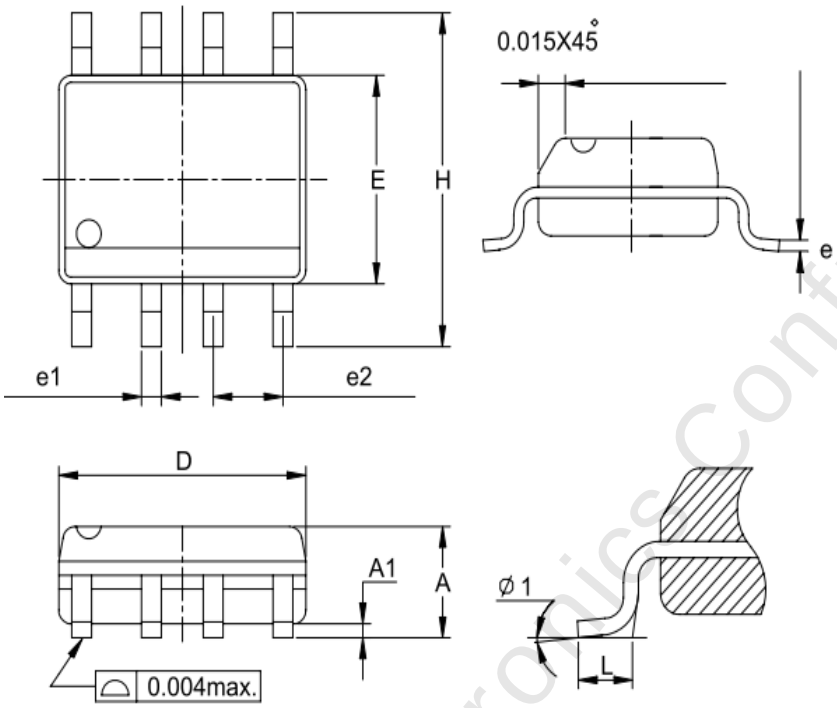
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

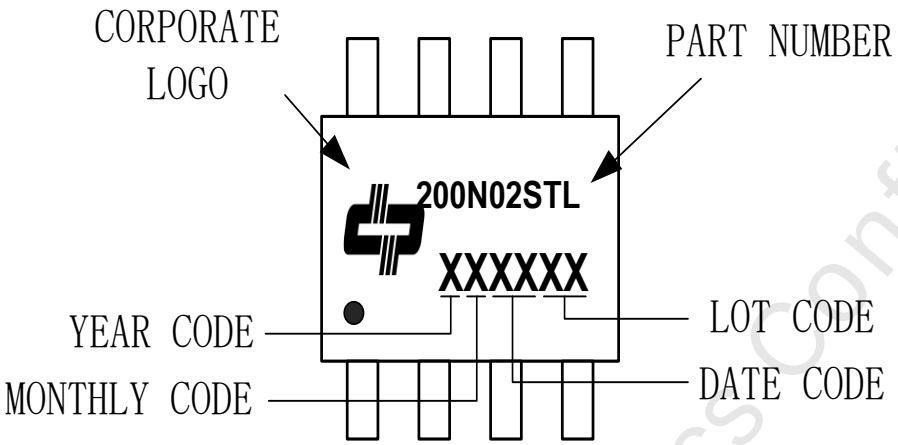


Package Outline: SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.5BSC	
Φ1	8°		8°	

Part Marking Information



Revision History

Revison	Major changes
1.0	Release for formal version1.0

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