Product Features

- Core and system
  - 32-bit ARM cortex-M0 core with single-cycle hardware multiplier
  - System frequency up to 48MHz
  - Cordic trigonometric and division acceleration unit
- Operating voltage range: 2.5V~5.5V
- Operating temperature range: -40°C~105°C
- Memory
  - Flash: 32KB
  - SRAM: 4KB
- Clock source:
  - HSI: 48MHz internal high-speed oscillator, clock accuracy of ±1% @25°C, ±2.5% @-40~105°C @5V
  - LSI: 32.768KHz internal low-speed oscillator
- Low power mode:
  - Support for idle, sleep, and stop modes. In stop mode, all peripheral register data and SRAM content are saved, and the low-power timer, watchdog, and GPIO input wake-up are supported.
- 12bit ADC
  - Maximum sampling rate: 1M sps
  - 16-bit hardware oversampling
  - PGA differential input
  - Number of channels: 10 external channels (including 3 channels with PGA), and 1 internal channel (temperature sensor)
  - Hardware-triggered ADC sampling
  - Separate storage of conversion results for all external channels
- 4 analog comparators
  - Equipped with hysteresis function
  - Adjustable reference voltage
  - Digital filtering and debounce
  - Adjustable comparator output polarity
  -Support for enabling embedded Back Electromotive Force (BEMF) resistors
- 3 Programmable Gain Amplifiers (PGA)
  - Differential input, single-ended output
  - Adjustable gain with built-in feedback resistor network
- Communication interface:
  - 2 UART channels
  - 1 SPI channel
  - 1 I2C channel
- Timer/counter/PWM
  - 1 16-bit EPWM timer: Supports 4 pairs of 8-channel PWM output, with complementary, dead time, and brake features
  - 2 16-bit Capture Compare Timers (CCT): Can be used as general-purpose timers or for motor control, supporting 2 input captures and output comparisons, as well as PWM output
  - 1 motor sensor interface timer, supporting HALL, quadrature encoder input, and input filtering
  - 3 general-purpose 32-bit timers (TIM)
  - 1 LPTIM low-power timer
  - 1 watchdog timer
- Fast GPIO
  - 32Pin package supports up to 28 IOs, 28Pin package supports up to 26 IOs, 24Pin package supports up to 22 IOs, and 20Pin package supports up to 18 IOs
  - Support for Open Drain
  - Configurable as output (push-pull or open-drain), input (floating, pull-up, or pull-down), or other dedicated functions
  - Maximum output current drive capacity of 20mA
- Peripheral interconnection matrix
  - Some peripherals can be triggered by hardware signals to run, thereby reducing operational latency and CPU load
- Debugging mode
  - Serial debugging interface (SWD)
- Packaging
  - TSSOP28、TSSOP20、SSOP24、LQFP32、QFN32

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Product Model

Series	Part Number	Core	Math Accelerator	Operating frequency(MHz)	Flash (KB)	RAM (KB)	GPIO	12bit ADC	ADC channels	ADC sampling rate(Msps)	PGA	ACMP	POSIF	EPWM	CCT	TIM	CRC	UART	I2C	SPI	Package
Value Line DPM32M03	DPM32M031G6P7	M0	Cordic, division unit	48	32	4	26	1	10	1	3	4	1	1	2	3	1	2	1	1	TSSOP28
	DPM32M031H6Q7	M0	Cordic, division unit	48	32	4	22	1	10	1	3	4	1	1	2	3	1	2	1	1	SSOP24
	DPM32M031F6P7	M0	Cordic, division unit	48	32	4	18	1	10	1	3	4	1	1	2	3	1	2	1	1	TSSOP20
	DPM32M031K6T7	M0	Cordic, division unit	48	32	4	28	1	10	1	3	4	1	1	2	3	1	2	1	1	LQFP32
	DPM32M031K6N7	M0	Cordic, division unit	48	32	4	28	1	10	1	3	4	1	1	2	3	1	2	1	1	QFN32

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Contents

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

1 Introduction

1.1 Overview

The product utilizes a high-performance 32-bit microcontroller (MCU) based on the ARM® Cortex™-M0 core, with a maximum system frequency of up to 48 MHz. It features a nested vector interrupt controller and includes various components such as parallel I/O ports (supporting general input, pull-up/pull-down input, push-pull output, open-drain output, and configurable edge or level-triggered interrupts), multiple timer combinations, SPI, I2C, UART, EPWM, CCT, trigonometric function (Cordic), hardware division unit, ADC, ACMP, and PGA.

2 Function Overview

2.1 Arm Cortex M0 Core

The Cortex®-M0 processor is an entry-level 32-bit Arm Cortex processor that offers higher code density than other 8-bit and 16-bit MCUs. It is characterized by high performance and low power consumption, with the core tightly coupled to a nested vector interrupt controller (NVIC).

2.2 Embedded Flash Memory (eFlash)

The embedded flash memory supports a main storage area of 32K Bytes and 1K Bytes of option Bytes. It supports read operations, page erase, full chip erase, and can be

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

programmed with 8/16/32-bit data. The Flash memory also supports read protection, erase/write protection, and configuration register write protection. Additionally, it features instruction prefetch and caching to accelerate instruction execution.

2.3 Embedded SRAM

The product includes 4K Bytes of embedded SRAM.

2.4 Nested Vector Interrupt Controller (NVIC)

The configurable NVIC is closely coupled with the processor core, capable of handling up to 32 maskable interrupt channels (excluding the 16 Cortex®-M0 interrupt lines) and 16 programmable priority levels.

Key features of the NVIC include:

- Low-latency interrupt processing
- Tightly coupled NVIC interface
- Early interrupt handling capability
- Direct interrupt vector entry address into the core
- Support for interrupt nesting, with higher priority interrupts preempting lower ones
- Interrupt tail-chaining functionality
- Automatic field recovery on interrupt return, eliminating the need for additional operations

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

2.5 Clock and Reset

The clock controller distributes clocks from various oscillators to the core and peripherals, manages clock gating in low-power modes, and ensures clock robustness.

The chip provides the following clock sources:

- High-speed internal clock (HSI RC) at 48 MHz
- Low-speed internal clock (LSI RC) at 32.768 KHz

HSI is used as the system clock, and the system clock is divided by two configurable frequency dividers to output the AHB and APB clocks.

LSI clock can be used as the clock source for LPTIM and WDG.

The chip supports Microcontroller Clock Output (MCO), allowing the clock to be output to the MCO pin, with selectable sources including HSI clock divided by 6 and LSI clock.

The chip features two types of resets: power reset and system reset.

Power reset sources include Power-On Reset (POR), Power-Down Reset (PDR), External Button Reset, and Power-On Safety Check Reset (which checks if the startup process has been maliciously attacked or heavily disturbed).

System resets include the following: software reset, CPU lockup reset (disabled by default, can be enabled by software), WDG system watchdog reset, and PVD voltage monitoring abnormal reset.

2.6 Power Supply Scheme

The VDD voltage range is 2.5V to 5.5V. The VDD pin supplies power to the I/O pins and

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

internal circuits.

2.7 Low Power Modes

The product supports three low-power modes: SLEEP, DEEP SLEEP, and STOP.

Refer to the table below for details.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Low Power Modes	SLEEP	DEEP SLEEP	STOP
Register RCC_LPM_CR	-	MODE=00	MODE=01
CM0 register SCB_SCR.SLEEPDEEP	0	1	1
Enter instruction	WFI or WFE	WFI or WFE	WFI or WFE
Wake-up source	Can be woken up by any interrupt	Can be woken up by any interrupt	Can be woken up by GPIO, LPTIM, or WDG interrupt
IO output state	Hold	Hold	Hold
SRAM, register	Hold	Hold	Hold
Definition	Only the CPU clock is turned off, all peripherals (including internal CPU peripherals such as NVIC, SysTick) continue to operate normally.	1. The CPU clock and internal CPU peripherals' clocks are turned off. 2. System peripheral clocks can be configured to be on or off in the RCC_SLEEP_CR register.	1. The CPU clock and internal CPU peripherals' clocks are turned off. 2. All system peripheral clocks are off except for the LSI low-speed clock, which can be configured. The software can choose to turn the LSI clock on or off in STOP mode by configuring the RCC_STOP_CR register. 3. The high-speed clock source HSI is off, and modules such as ADC, ACMP and PVD are also turned off. 4. Flash enters Deep Standby mode.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Post-wake status	The MCU returns to normal operation mode, and the program continues to execute.	The MCU returns to normal operation mode, and the program continues to execute.	The MCU returns to normal operation mode, and the program continues to execute.
Notes	-	If the UART/SPI/IIC clocks are configured to be off in Deep Sleep mode, the software should disable these peripherals before entering this mode.	If the LSI clock is configured to be off in Stop mode, the LPTIM counter value will be reset. The software should disable UART/SPI/IIC before entering Stop mode.

2.8 Programmable Voltage Detector (PVD)

The embedded Programmable Voltage Detector (PVD) is used to monitor the VDD supply voltage and compare it with a software-configurable voltage threshold. The internal voltage comparator generates a transition signal, and the software can be set to trigger an interrupt or reset on the falling, rising, or high/low transitions of the transition signal. The main features of the PVD include:

- Programmable threshold voltage: 2.2V, 2.4V, 2.6V, 2.8V, 3.0V, 3.2V, 3.4V, 3.6V, 3.8V, 4.0V
- Support for digital filtering and debounce of comparator output signal
- Support for four event trigger types: rising edge, falling edge, high level, and low level
- Configurable to trigger asynchronous interrupt or reset on event

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

2.9 Peripheral interconnection matrix

Multiple peripherals within the MCU are directly connected, supporting hardware mutual triggering. This triggering method eliminates software delays and, once configured, does not require software intervention, thus saving CPU resources. These interconnections can operate in both normal and low-power modes, depending on the peripheral. The connection relationships are as follows:

Source Peripheral Event	Target Peripheral				
	ADC	CCT0	CCT1	POSIF	EPWM
IO trigger (ADC_TRIG)	Y				
EPWM ADC compare event 1	Y				
EPWM ADC compare event 2	Y				
TIM0 count completion event	Y				
TIM1 count completion event	Y				
ACMP 0 output		Y	Y	Y	Y
ACMP 1 output		Y	Y	Y	Y
ACMP 2 output		Y	Y	Y	Y
ACMP 3 output		Y	Y	Y	Y

2.10 Cyclic Redundancy Check Unit (CRC)

The Cyclic Redundancy Check (CRC) unit calculates CRC codes based on a specified polynomial and 8, 16, or 32-bit data, commonly used to verify the integrity of data transmission or storage.

- Optional CRC-32 polynomial: 0x4C11DB7

  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Optional CRC-16 polynomial: 0x1021 $X^{16} + X^{12} + X^5 + 1$

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

- Optional CRC-16 polynomial: 0x8005 $X^{16} + X^{15} + X^2 + 1$
- Support for 8, 16, and 32-bit data input widths
- CRC calculations for 32-bit data in 4 AHB clock cycles
- Input data and output results can be inverted
- Configurable initial value for CRC

2.11 General Purpose IO (GPIO)

The product supports up to 28 general-purpose input/output pins (GPIO), including ports PA, PB, and PD.

Each port has a corresponding set of configuration and status registers, allowing users to flexibly configure each IO as general-purpose input/output, peripheral multiplexing function (AF), or analog function according to application requirements.

It supports GPIO interrupts triggered by rising edge, falling edge, both edges, and high/low level.

Each GPIO pin can be flexibly configured with pull-up, pull-down, or no pull resistance. Digital output supports push-pull and open-drain selection, with up to four selectable output speeds.

2.12 Cordic and Division Unit (Math Accelerator)

The embedded hardware Coordinate Rotation Digital Computer (Cordic) and division unit can be used to accelerate motor control algorithms, reducing CPU resource usage. The hardware Cordic calculation unit supports cosine and sine calculations, as well as calculation

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

of inverse tangent and modulus values for given cosine and sine values, all in Q15 format. The hardware division unit supports Q15 format division, where the dividend (16-bit signed) is left-shifted by 15 bits and divided by the divisor (16-bit signed), with overflow protection.

2.13 Timer （TIM）

The 32-bit general-purpose timer supports a 32-bit auto-reload value and down-counting. It triggers an interrupt when the count value reaches zero from the set value. The timer supports both one-time and periodic counting modes.

2.14 Capture Compare Timer (CCT)

The Capture Compare Timer features a 16-bit up-counter supporting two counting modes: single-pulse counting and periodic counting. The counting clock is derived from a prescaler-divided clock. The internal timer supports two operating modes: Capture Input mode and Compare Output mode. The Capture Input mode allows for input filtering and edge detection, while the Compare Output mode can output edge-aligned PWM signals.

Key features:

- 16-bit up-counter with a 16-bit auto-reload register
- Two independent channels, each configurable for a specific operating mode
- Two operating modes: Capture Input and Compare Output
- PWM generation (edge-aligned mode)
- Single-pulse mode output
- Prescaler (1/2/4/8/16/32/64/128)

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

- Input filtering and edge detection

2.15 Enhanced PWM Timer (EPWM)

Enhanced Pulse Width Modulation (EPWM) supports 4 output channels, with 3 channels supporting 6 complementary PWM outputs with dead-time insertion. Key features:

- Equipped with a 16-bit counter, supporting both up/down counting (center-aligned mode) and up counting modes
- Supports both single pulse counting and periodic counting modes
- Supports counting clock frequency division factors 1/2/4/8/16/32/64/128
- Supports 4-channel PWM generation, with 3 channels supporting 3 pairs of complementary (6-way) PWM signals, and PWM phase shifting
- Supports dead-time insertion
- Supports force change of I/O output state
- Supports generation of 2 synchronized trigger signals for ADC sampling, with the same timing reference as PWM
- Supports multiple hardware emergency stop signals, with hardware filtering and polarity selection for emergency stop signals. The I/O output state after an emergency stop can be configured

2.16 Hall and Encoder Interface Controller (POSIF)

POSIF can capture encoder or Hall sensor inputs, performing hardware parsing of input signals and automatic counting. It can be used in motor control to obtain the operational

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

status of the motor.

Key features:

- Configurable in two modes: encoder and Hall sensor
- Configurable counting prescaler (1/2/4/8/16/32/64/128)
- 3-way input signal filtering, with the option to use the output of the analog comparator as input
- 16-bit encoder counter, supporting quadrature counting and direction counting
- Quadrature encoder supporting automatic reset of the count value upon Z-phase input
- Quadrature encoder supporting setting a maximum count value. When counting down to 0, the hardware automatically adjusts to the maximum count value
- Encoder supporting a 23-bit input pulse counter for counting the number of input pulses
- 23-bit Hall width counter, automatically capturing edge changes of the input, with configurable interrupt generation on edge change
- Configurable maximum Hall width, generating an interrupt when the maximum value is exceeded

2.17 Low Power Timer (LPTIM)

LPTIM includes a 32-bit up-counter that uses a 32KHz low-frequency clock as the counting clock and can periodically trigger interrupts. It can also serve as an MCU wake-up

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

source in low power modes.

2.18 Watchdog (WDG)

The watchdog peripheral offers high safety, accurate timing, and flexible usage.

It detects and resolves faults caused by software errors and triggers a system reset when the counter reaches a predefined timeout value.

2.19 Inter-Integrated Circuit Interface (I2C)

The I2C interface implements I2C timing sequences, transmission protocols, arbitration decisions, and event interrupts in hardware, providing multi-master communication capabilities. This module can operate as a master or slave on a multi-master I2C bus and supports standard, fast, and high-speed transmission modes. When I2C is enabled, the corresponding GPIO for SCL and SDA should be configured in open-drain mode and pulled up externally with resistors.

Key features:

- Optional master and slave modes
- Standard mode (up to 100 Kbit/s)
- Fast mode (up to 400 Kbit/s)
- High-speed mode (up to 1 Mbit/s)
- 7-bit and 10-bit addressing modes
- Broadcast call function
- Programmable SDA data setup and hold time

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

- Bus event management
- Multi-master communication
- SCL pull-down to control communication speed
- Digital filtering of input signals
- Communication timeout monitoring
- 1-byte receive/transmit buffer

2.20 Universal Asynchronous Receiver/Transmitter (UART)

The UART enables flexible full-duplex data exchange with external devices. The internal programmable baud rate generator supports various baud rates to meet the requirements of external devices for the industry-standard non-return-to-zero (NRZ) asynchronous serial data format.

Key features:

- Full-duplex asynchronous communication
- NRZ standard format
- Programmable transmit and receive baud rates
- Programmable data word length (6-bit, 7-bit, 8-bit, or 9-bit)
- Programmable data transmission sequence, with MSB or LSB first
- Configurable stop bits (support for 1 or 2 stop bits)
- Single-wire half-duplex communication
- Independent enable for data transmission and reception

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

- Data transmission/reception interrupts and error detection interrupts
- Parity check

2.21 Serial Peripheral Interface (SPI)

The SPI interface is widely used for communication between the MCU and external devices, supporting full-duplex and half-duplex synchronous serial communication. The software-controlled chip select signals can achieve a communication network structure of one master and multiple slaves.

Key features:

- Master or slave operation mode
- Full-duplex synchronous transmission
- Simplex synchronous transmission
- Programmable data length from 4 to 16 bits
- Software or hardware NSS (chip select) management
- Programmable clock polarity and phase
- Programmable data order, supporting MSB-first or LSB-first
- In master mode, support for a maximum clock frequency of 24 MHz for transmission and 12 MHz for reception
- In slave mode, support for a maximum clock frequency of 8 MHz
- Support for data transmission/reception interrupts
- Support for transmission error interrupts

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

2.22 Analog-to-Digital Converter (ADC)

The ADC is a 12-bit successive approximation analog-to-digital converter capable of sampling 11 analog input channels, including one internal channel for measuring the internal temperature sensor, and 10 external analog input channels. The ADC unit supports single-channel single acquisition, single-channel continuous acquisition, and sequential scanning acquisition modes. Each mode has an independent 16-bit data register, and the acquired data is stored in either left-aligned or right-aligned format. It also supports analog watchdog (signal window voltage monitoring) and hardware oversampling, which effectively reduces the CPU's computational burden for signal monitoring and oversampling data processing. Additionally, the ADC module supports channel queue jumping data acquisition to obtain channel conversion data in a timely manner in continuous or scan modes.

2.23 Temp Sensor

The Temp Sensor is built into the device and can be used to measure the device's junction temperature (TJ). The Temp Sensor's analog output is connected to input channel 14 of the ADC, and the software can sample temperature data through the ADC. The output voltage of the Temp Sensor varies linearly with temperature, and this linear offset varies depending on the chip's process. To improve the accuracy of the Temp Sensor, the ADC performs offset error calibration on the Temp Sensor's sampling channel.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

2.24 Internal Voltage Reference (VREF)

Upon power-up, the device can provide reference voltage to internal analog devices (such as ADC, ACMP, and PGA).

The internal voltage reference offers two levels: operating voltage (VDD) and 2.4V internal bandgap reference voltage.

2.25 Analog Comparator (ACMP)

The device includes four analog comparators (ACMP) that can be used for low-power wake-up triggered by analog signals, analog signal conditioning, and other functions.

Key features:

- ACMP positive terminal input selection: CMP_IN0-5, PGA0, and PGA1 outputs
- ACMP negative terminal input selection: CMP_IN0-5, Vref divider, and DAC output (DAC is only used to generate ACMP negative terminal input voltage)
- Digital filtering and debounce
- Adjustable comparator output polarity
- Asynchronous interrupts
- Hysteresis function
- Comparator output to the interconnect matrix
- Support for enabling embedded Back Electromotive Force (BEMF) resistors

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

2.26 Programmable Gain Amplifier (PGA)

The device includes three programmable gain amplifiers, each supporting differential input via analog pins with built-in feedback resistors to set the operational amplifier gain. The outputs of the three amplifiers (PGA0/1/3) can be connected to ADC channels 0/1/3, and the outputs of PGA0 and PGA1 can also serve as inputs to the analog comparators (ACMP). Key features:

- Differential input
- Configurable gain ranging from 1, 2, 4, 8, 16, 32
- Internal connection of PGA0/1/3 output to ADC analog input
- Internal connection of PGA0 and PGA1 output to ACMP

Note: When the PGA sampling port may generate a negative voltage, it is recommended to connect a 20KΩ resistor in series at the input end.

2.27 Device Electronic Signature

The device retains an electronic signature, which is a read-only memory unit that can be read through the debugging interface or by the CPU. It contains a 96-bit unique identification code, package type, Flash and RAM size information, and supports byte (8-bit), half-word (16-bit), and full-word (32-bit) access. All information is factory-set and cannot be modified by the user.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

2.28 Debug Support

The product supports a two-wire serial debug port (SW-DP).

When the MCU is in low power mode, the debugger can wake up the MCU by initiating a connection through the SWD port, allowing access to the core and peripheral registers via SWD without any restrictions on standard debugging functions.

When the MCU is already in debug mode, it cannot enter low power mode.

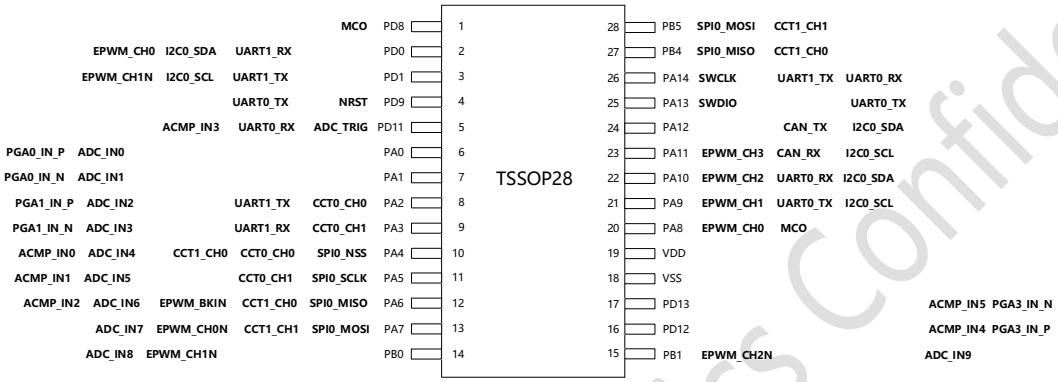
During breakpoint or single-step debugging, the DBG_CFG register can be configured to decide whether to pause the counter peripherals (EPWM, CCT, TIM, WDG, and LPTIM) from counting.

Developer Microelectronics Confidential

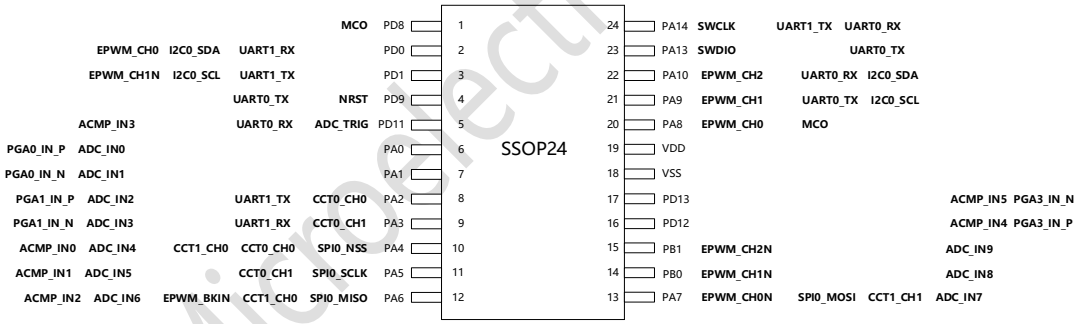
The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3 Pinouts and Pin Descriptions

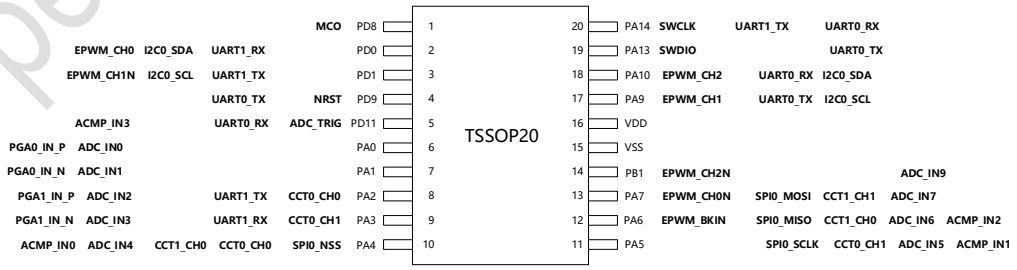
3.1 DPM32M031G6P7 Pinout Diagram



3.2 DPM32M031H6Q7 Pinout Diagram



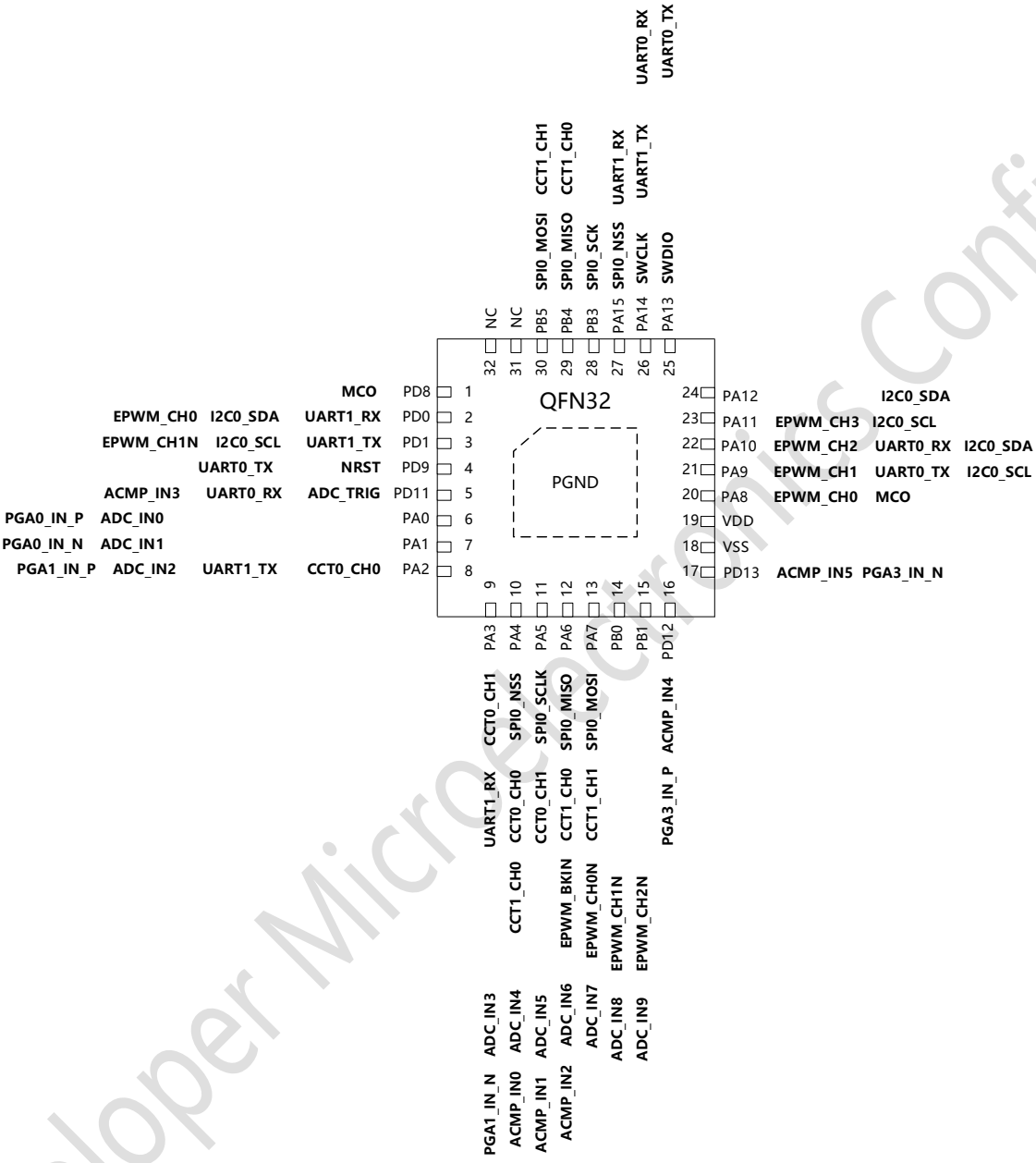
3.3 DPM32M031F6P7 Pinout Diagram



Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

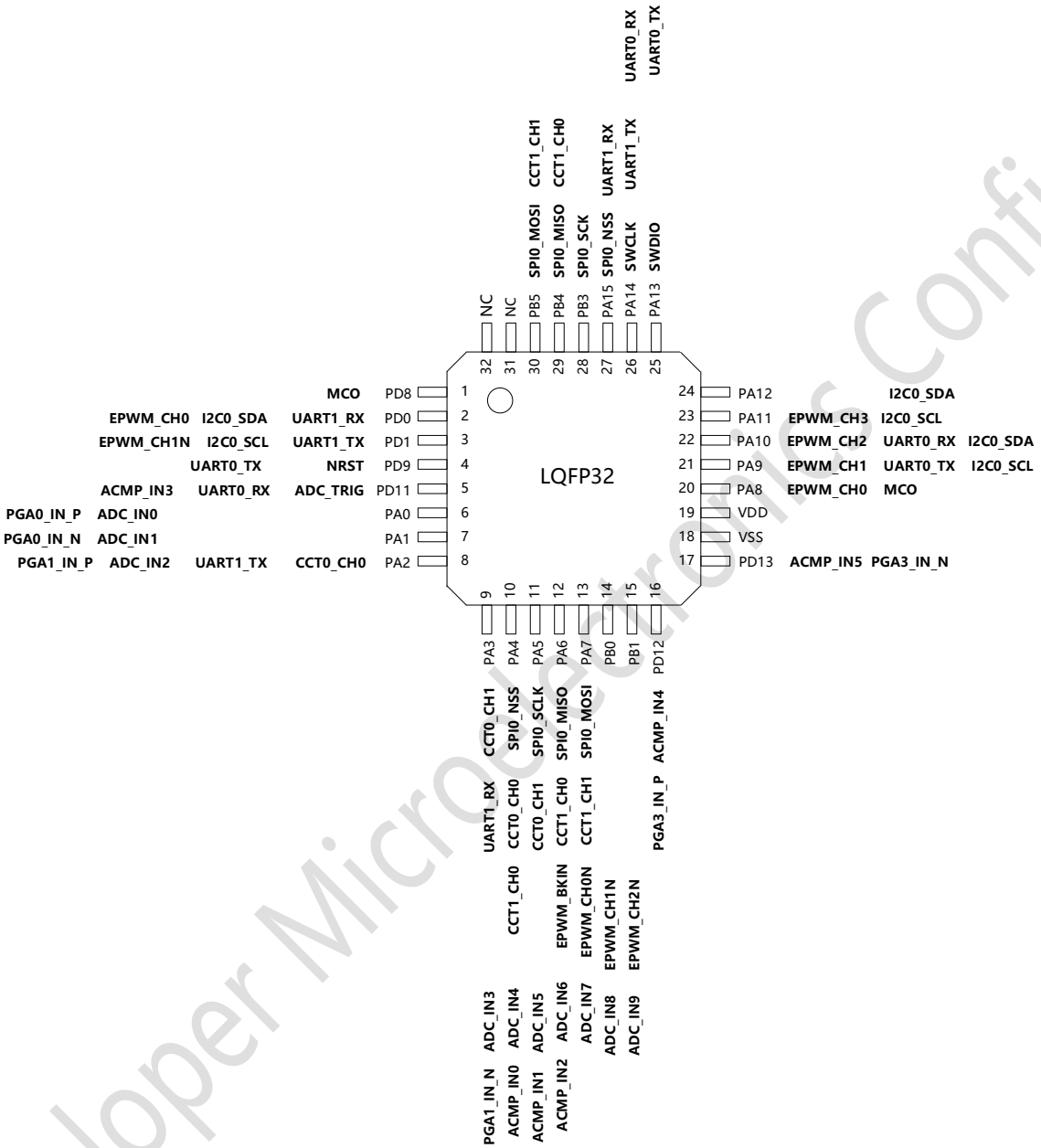
3.4 DPM32M031K6N7 Pinout Diagram



Developer MicroElectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3.5 DPM32M031K6T7 Pinout Diagram



Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3.6 DPM32M031G6P7, DPM32M031H6Q7 and DPM32M031F6P7

Pin Multiplexing Table

DPM32M031G6P7	DPM32M031H6Q7	DPM32M031F6P7	Digital Alternate Function	Analog Alternate Function	Default Function
PA0	PA0	PA0		ADC_IN0、PGA0_IN0	Input Mode
PA1	PA1	PA1		ADC_IN1、PGA0_IN1	Input Mode
PA2	PA2	PA2	UART1_TX/CCT0_CH0	ADC_IN2、PGA1_IN0	Input Mode
PA3	PA3	PA3	UART1_RX/CCT0_CH1	ADC_IN3、PGA1_IN1	Input Mode
PA4	PA4	PA4	SPI0_NSS/CCT0_CH0/CCT1_CH0	ADC_IN4、ACMP_IN0	Input Mode
PA5	PA5	PA5	SPI0_SCK/CCT0_CH1	ADC_IN5、ACMP_IN1	Input Mode
PA6	PA6	PA6	CCT1_CH0/SPI0_MISO/EPWM_BKIN	ADC_IN6、ACMP_IN2	Input Mode
PA7	PA7	PA7	CCT1_CH1/SPI0_MOSI/EPWM_CH0N	ADC_IN7	Input Mode
PA8	PA8		MCO/EPWM_CH0		Input Mode
PA9	PA9	PA9	UART0_TX/EPWM_CH1/I2C0_SCL		Input Mode
PA10	PA10	PA10	UART0_RX/EPWM_CH2/I2C0_SDA		Input Mode
PA11			EPWM_CH3/I2C0_SCL		Input Mode
PA12			I2C0_SDA		Input Mode
PA13	PA13	PA13	SWDIO/UART0_TX		SWDIO,Pullup
PA14	PA14	PA14	UART1_TX/SWCLK/UART0_RX		SWCLK,Pulldown
PB0	PB0		EPWM_CH1N	ADC_IN8	Input Mode
PB1	PB1	PB1	EPWM_CH2N	ADC_IN9	Input Mode
PB4			CCT1_CH0/SPI0_MISO		Input Mode
PB5			CCT1_CH1/SPI0_MOSI		Input Mode
PD0	PD0	PD0	I2C0_SDA/UART1_RX/EPWM_CH0		Input Mode
PD1	PD1	PD1	I2C0_SCL/UART1_TX/EPWM_CH1N		Input Mode
PD8	PD8	PD8	MCO		In Mode,Pulldown
PD9	PD9	PD9	UART0_TX/NRST		NRST,Pullup
PD11	PD11	PD11	UART0_RX/ADC_TRIG	ACMP_IN3	Input Mode
PD12	PD12			PGA3_IN0、ACMP_IN4	Input Mode
PD13	PD13			PGA3_IN1、ACMP_IN5	Input Mode

Note: POSIF_CH0, POSIF_CH1, and POSIF_CH2 share the same digital multiplexing function with CCT0_CH0, CCT0_CH1, and CCT1_CH0, respectively. When using POSIF (Hall and Encoder Interface), the corresponding IOs should be configured as CCT channel multiplexing functions according to this mapping.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3.7 DPM32M031K6N7 Pin Multiplexing Table

DPM32M031K6N7	Digital Alternate Function	Analog Alternate Function	Default Function
PA0		ADC_IN0、PGA0_IN0	Input Mode
PA1		ADC_IN1、PGA0_IN1	Input Mode
PA2	UART1_TX/CCT0_CH0	ADC_IN2、PGA1_IN0	Input Mode
PA3	UART1_RX/CCT0_CH1	ADC_IN3、PGA1_IN1	Input Mode
PA4	SPI0_NSS/CCT0_CH0/CCT1_CH0	ADC_IN4、ACMP_IN0	Input Mode
PA5	SPI0_SCK/CCT0_CH1	ADC_IN5、ACMP_IN1	Input Mode
PA6	CCT1_CH0/SPI0_MISO/EPWM_BKIN	ADC_IN6、ACMP_IN2	Input Mode
PA7	CCT1_CH1/SPI0_MOSI/EPWM_CH0N	ADC_IN7	Input Mode
PA8	MCO/EPWM_CH0		Input Mode
PA9	UART0_TX/EPWM_CH1/I2C0_SCL		Input Mode
PA10	UART0_RX/EPWM_CH2/I2C0_SDA		Input Mode
PA11	EPWM_CH3/CAN_RX/I2C0_SCL		Input Mode
PA12	CAN_TX/I2C0_SDA		Input Mode
PA13	SWDIO/UART0_TX		SWDIO,Pullup
PA14	UART1_TX/SWCLK/UART0_RX		SWCLK,Pulldown
PA15	UART1_RX/SPI0_NSS		Input Mode
PB0	EPWM_CH1N	ADC_IN8	Input Mode
PB1	EPWM_CH2N	ADC_IN9	Input Mode
PB3	SPI0_SCK		Input Mode
PB4	CCT1_CH0/SPI0_MISO		Input Mode
PB5	CCT1_CH1/SPI0_MOSI		Input Mode
PD0	I2C0_SDA/UART1_RX/EPWM_CH0		Input Mode
PD1	I2C0_SCL/UART1_TX/EPWM_CH1N		Input Mode
PD8	MCO		In Mode,Pulldown
PD9	UART0_TX/NRST		NRST,Pullup
PD11	UART0_RX/ADC_TRIG	ACMP_IN3	Input Mode
PD12		PGA3_IN0、ACMP_IN4	Input Mode
PD13		PGA3_IN1、ACMP_IN5	Input Mode

Note: POSIF_CH0, POSIF_CH1, and POSIF_CH2 share the same digital multiplexing function with CCT0_CH0, CCT0_CH1, and CCT1_CH0, respectively. When using POSIF (Hall and Encoder Interface), the corresponding IOs should be configured as CCT channel multiplexing functions according to this mapping.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3.8 DPM32M031K6T7 Pin Multiplexing Table

DPM32M031K6T7	Digital Alternate Function	Analog Alternate Function	Default Function
PA0		ADC_IN0、PGA0_IN0	Input Mode
PA1		ADC_IN1、PGA0_IN1	Input Mode
PA2	UART1_TX/CCT0_CH0	ADC_IN2、PGA1_IN0	Input Mode
PA3	UART1_RX/CCT0_CH1	ADC_IN3、PGA1_IN1	Input Mode
PA4	SPI0_NSS/CCT0_CH0/CCT1_CH0	ADC_IN4、ACMP_IN0	Input Mode
PA5	SPI0_SCK/CCT0_CH1	ADC_IN5、ACMP_IN1	Input Mode
PA6	CCT1_CH0/SPI0_MISO/EPWM_BKIN	ADC_IN6、ACMP_IN2	Input Mode
PA7	CCT1_CH1/SPI0_MOSI/EPWM_CH0N	ADC_IN7	Input Mode
PA8	MCO/EPWM_CH0		Input Mode
PA9	UART0_TX/EPWM_CH1/I2C0_SCL		Input Mode
PA10	UART0_RX/EPWM_CH2/I2C0_SDA		Input Mode
PA11	EPWM_CH3/CAN_RX/I2C0_SCL		Input Mode
PA12	CAN_TX/I2C0_SDA		Input Mode
PA13	SWDIO/UART0_TX		SWDIO,Pullup
PA14	UART1_TX/SWCLK/UART0_RX		SWCLK,Pulldown
PA15	UART1_RX/SPI0_NSS		Input Mode
PB0	EPWM_CH1N	ADC_IN8	Input Mode
PB1	EPWM_CH2N	ADC_IN9	Input Mode
PB3	SPI0_SCK		Input Mode
PB4	CCT1_CH0/SPI0_MISO		Input Mode
PB5	CCT1_CH1/SPI0_MOSI		Input Mode
PD0	I2C0_SDA/UART1_RX/EPWM_CH0		Input Mode
PD1	I2C0_SCL/UART1_TX/EPWM_CH1N		Input Mode
PD8	MCO		In Mode,Pulldown
PD9	UART0_TX/NRST		NRST,Pullup
PD11	UART0_RX/ADC_TRIG	ACMP_IN3	Input Mode
PD12		PGA3_IN0、ACMP_IN4	Input Mode
PD13		PGA3_IN1、ACMP_IN5	Input Mode

Note: POSIF_CH0, POSIF_CH1, and POSIF_CH2 share the same digital multiplexing function with CCT0_CH0, CCT0_CH1, and CCT1_CH0, respectively. When using POSIF (Hall and Encoder Interface), the corresponding IOs should be configured as CCT channel multiplexing functions according to this mapping.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3.9 PA Pin Digital Function Multiplexing Table

	Digital Alternate Function							
PIN	0	1	2	3	4	5	6	7
PA0								
PA1								
PA2	CCT0_CH0	UART1_TX						
PA3	CCT0_CH1	UART1_RX						
PA4	SPI0_NSS		CCT0_CH0	CCT1_CH0				
PA5	SPI0_SCK		CCT0_CH1					
PA6	SPI0_MISO	CCT1_CH0	EPWM_BKIN					
PA7	SPI0_MOSI	CCT1_CH1	EPWM_CH0N					
PA8	MCO		EPWM_CH0					
PA9		UART0_TX	EPWM_CH1		I2C0_SCL			
PA10		UART0_RX	EPWM_CH2		I2C0_SDA			
PA11			EPWM_CH3			I2C0_SCL		
PA12						I2C0_SDA		
PA13	SWDIO		UART0_TX					
PA14	SWCLK	UART1_TX	UART0_RX					
PA15	SPI0_NSS	UART1_RX						

3.10 PB Pin Digital Function Multiplexing Table

	Digital Alternate Function							
PIN	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PB0			EPWM_CH1N					
PB1			EPWM_CH2N					
PB2	EPWM_CH3N							
PB3	SPI0_SCK							
PB4	SPI0_MISO	CCT1_CH0						
PB5	SPI0_MOSI	CCT1_CH1						
PB6	UART0_TX	I2C0_SCL						
PB7	UART0_RX	I2C0_SDA						
PB8		I2C0_SCL						
PB9		I2C0_SDA						
PB10		I2C0_SCL						
PB11		I2C0_SDA						
PB12			EPWM_BKIN					
PB13			EPWM_CH0N					
PB14		CCT0_CH0	EPWM_CH1N					
PB15		CCT0_CH1	EPWM_CH2N					

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3.11 PD Pin Digital Function Multiplexing Table

	Digital Alternate Function							
PIN	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD0	UART1_RX	I2C0_SDA	EPWM_CH0					
PD1	UART1_TX	I2C0_SCL	EPWM_CH1N					
PD2								
PD3								
PD4	I2C0_SCL							
PD5	I2C0_SDA							
PD6								
PD7								
PD8	MCO							
PD9	NRST	UART0_TX						
PD10								
PD11	ADC_TRIG	UART0_RX						
PD12								
PD13								

3.12 Pin Analog Function Multiplexing Table

	Analog Alternate Function			
PIN	**0**	**1**	**2**	**3**
PA0	ADC_IN0	PGA0_IN0		
PA1	ADC_IN1	PGA0_IN1		
PA2	ADC_IN2	PGA1_IN0		
PA3	ADC_IN3	PGA1_IN1		
PA4	ADC_IN4	ACMP_IN0		
PA5	ADC_IN5	ACMP_IN1		
PA6	ADC_IN6	ACMP_IN2		
PA7	ADC_IN7			
PB0	ADC_IN8			
PB1	ADC_IN9			
PB10	PGA2_IN0			
PB11	PGA2_IN1			
PD11		ACMP_IN3		
PD12	PGA3_IN0	ACMP_IN4		
PD13	PGA3_IN1	ACMP_IN5		

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

3.13 Storage Mapping

3.13.1 System Storage Space Mapping

Start Address	End Address	Size	Address Assignment
0x0000_0000	0x0FFF_FFFF	128MB	Remapping space
0x1000_0000	0x1000_17FF	6KB	Reserved
0x1000_1800	0x1000_1BFF	1KB	User Option Bytes
0x1000_1C00	0x17FF_FFFF		Reserved
0x1800_0000	0x1800_7FFF	32KB	Embedded Flash (eFlash)
0x1800_8000	0x1801_FFFF		Reserved
0x1802_0000	0x1FFF_FFFF		Reserved
0x2000_0000	0x2000_0FFF	4KB	SRAM
0x2000_1000	0x2000_3FFF		Reserved
0x2000_4000	0x3FFF_FFFF		Reserved
0x4000_0000	0x4007_FFFF	512KB	128 x 4KB APB peripherals
0x4008_0000	0x400F_FFFF	512KB	128 x 4KB APB peripherals
0x4010_0000	0xDFFF_FFFF		Reserved
0xE000_0000	0xE00F_FFFF	1MB	Cortex-M0 peripherals
0xE010_0000	0xFFFF_FFFF		Reserved

3.13.2 APB Mapping

Classification	Start Address	Size	Address Assignment
System control	0x40001000	4KB	Reset and Clock Control (RCC), DEBUG Control, PGA Control
	0x40002000	4KB	Reserved
	0x40003000	4KB	System ROM table
	0x40004000	4KB	Reserved
	0x40005000	4KB	Reserved
	0x40006000	4KB	Reserved
	0x40007000	4KB	Reserved
Low-speed peripheral	0x40008000	4KB	UART0
	0x40009000	4KB	UART1

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

interface	0x4000A000	4KB	Reserved
	0x4000B000	4KB	Reserved
	0x4000C000	4KB	Reserved
	0x4000D000	4KB	Reserved
	0x4000E000	4KB	SPI0
	0x4000F000	4KB	Reserved
	0x40010000	4KB	Reserved
	0x40011000	4KB	Reserved
	0x40012000	4KB	I2C
	0x40013000	4KB	Reserved
	0x40014000	4KB	Reserved
	0x40015000	4KB	Reserved
	0x40016000	4KB	Reserved
	0x40017000	4KB	Reserved
	0x40018000	4KB	Reserved
Timer	0x40019000	4KB	TIM0
	0x4001A000	4KB	TIM1
	0x4001B000	4KB	TIM2
	0x4001C000	4KB	Reserved
	0x4001D000	4KB	Reserved
	0x4001E000	4KB	Reserved
	0x4001F000	4KB	CCT0
	0x40020000	4KB	CCT1
	0x40021000	4KB	Reserved
	0x40022000	4KB	Reserved
	0x40023000	4KB	EPWM
	0x40024000	4KB	Reserved
	0x40025000	4KB	Reserved
	0x40026000	4KB	Reserved
	0x40027000	4KB	WDG
	0x40028000	4KB	Reserved
	0x40029000	4KB	POSIF (HALL/encoder)
	0x4002A000	4KB	Reserved
	0x4002B000	4KB	Reserved
	0x4002C000	4KB	Reserved
	0x4002D000	4KB	LPTIM
Analog peripheral	0x40033000	4KB	SAR ADC
	0x40034000	4KB	Reserved

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

	0x40035000	4KB	DAC (only used to generate ACMP negative reference voltage)
	0x40036000	4KB	Reserved
	0x40037000	4KB	Reserved
	0x40038000	4KB	Reserved
	0x40039000	4KB	PVD
	0x4003A000	4KB	ACMP
	0x4003B000	4KB	Reserved
Others	0x4003C000	4KB	CRC
	0x4003D000	4KB	Reserved

3.13.3 AHB Mapping

Classification	Start Address	Size	Address Assignment
GPIOs	0x40080000	4KB	GPIO A
	0x40081000	4KB	GPIO B
	0x40082000	4KB	Reserved
	0x40083000	4KB	GPIO D
	0x40084000	4KB	Reserved
	0x40085000	4KB	Reserved
	0x40086000	4KB	Reserved
	0x40087000	4KB	Reserved
Computational accelerator	0x40088000	4KB	MATH_ACC (hardware Cordic and division unit)
eFlash controller	0x40089000	4KB	Embedded Flash controller
Reserved	0x4008A000	4KB	Reserved
	0x4008B000	4KB	Reserved
	0x4008C000	4KB	Reserved
	0x4008D000	4KB	Reserved
	0x4008E000	4KB	Reserved
	0x4008F000	4KB	Reserved

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

The load applied to the device should not exceed the values listed under "Absolute Maximum Ratings"; otherwise, it may cause permanent damage to the device. These ratings give the load limits only and do not imply error-free functional operation of the device under these conditions. Prolonged operation at maximum rating conditions may affect device reliability.

Symbol	Description	Min Value	Max Value	Unit
V_{DD} - V_{SS}	External main supply voltage(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	Vss-0.3	5.5	V

1. All power and ground pins must always be connected to the external power supply system within the allowable range.

2. $I_{INJ(PIN)}$ must not exceed its limits, which ensures V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed to stay within its maximum value, then external measures must limit $I_{INJ(PIN)}$ to not exceed its maximum value. When $V_{IN} > V_{DD}$, a positive injection current occurs; when $V_{IN} < V_{SS}$, a negative injection current occurs.

Symbol	Description	Max Value	Unit
I_{VDD}	Total current through V_{DD} power line (supply current)(1)	100	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current)(1)	100	mA
I_{IO}	Output sink current on any I/O and control pins	20	mA
	Output current on any I/O and control pins	-20	mA

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

	Injection current on other pins(4)	±5	mA
$\sum I_{INJ(PIN)}$	Total injection current on all I/O and control pins(4)	±5	mA

1. All power and ground pins must always be connected to the external power supply system within the allowable range.

2. $I_{INJ(PIN)}$ must not exceed its limits, which ensures V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed to stay within its maximum value, then external measures must limit $I_{INJ(PIN)}$ to not exceed its maximum value. When $V_{IN} > V_{DD}$, a positive injection current occurs; when $V_{IN} < V_{SS}$, a negative injection current occurs.

3. Reverse injection current may interfere with the device's analog performance.

4. When multiple I/O ports simultaneously have injection current, the maximum value of $\sum I_{INJ(PIN)}$ is the instantaneous absolute sum of positive and negative injection currents. This result is based on the characteristic of maximum $\sum I_{INJ(PIN)}$ values across all I/O ports of the device.

4.2 Operating Conditions

4.2.1 General Operating Conditions

Symbol	Parameter	Condition	Min Value	Max Value	Unit
V_{DD}	External input voltage range		2.5	5.5	V
f_{HCLK}	Internal AHB clock frequency			48	MHz
f_{PCLK}	Internal APB clock frequency			48	MHz
T_A	Ambient temperature		-40	105	℃

4.2.2 Power-Up and Power-Down Operating Conditions

The parameters given in the table below are tested under general operating conditions.

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

Symbol	Parameter	Condition	Min Value	Max Value	Unit
t_{VDD}	V_{DD} rising rate		200	∞	us/V
	V_{DD} falling rate		20	∞	

4.2.3 Characteristics of Embedded Reset and Power Control Module

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit
V_{por}	POR release voltage (power-up process)			2.05		V
	BOR detection voltage (power-down process)			2		
$T_{RSTTEMPO}$	Reset duration			10		ms
V_{PVD}	Level selection of programmable voltage detector	PLS[3:0] =0010	2.182	2.2	2.212	V
		PLS[3:0] =0011	2.39	2.4	2.416	V
		PLS[3:0] =0100	2.59	2.6	2.619	V
		PLS[3:0] =0101	2.79	2.8	2.822	V
		PLS[3:0] =0110	2.989	3.0	3.024	V
		PLS[3:0] =0111	3.189	3.2	3.227	V
		PLS[3:0] =1000	3.388	3.4	3.428	V
		PLS[3:0] =1001	3.588	3.6	3.63	V
		PLS[3:0] =1010	3.788	3.8	3.832	V
		PLS[3:0] =1011	3.987	4.0	4.034	V

4.2.4 Supply Current Characteristics

Power consumption is influenced by various parameters and factors, including operating voltage, ambient temperature, I/O pin loads, product software configuration, operating frequency, I/O pin flipping rate, the location of the program in memory, and the code being executed.

Microcontroller conditions:

(1) All I/O pins are in input mode and connected to a static level—VSS (no

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

load).

(2) All peripherals are turned off unless otherwise noted.

(3) Flash memory access time is adjusted according to the frequency of f_{HCLK}.

(4) When peripherals are enabled: $f_{PCLK} = f_{HCLK}$.

(5) VDD=5V.

(6) It operates at room temperature.

Typical current consumption in Run, SLEEP, and DEEP SLEEP modes

Symbol	Condition				Typical Value		Unit
	Mode	General	f_{HCLK}	Fetch from	Enable All Peripherals	Disable All Peripherals	
I_{DD}	Run	Internal clock source	48M	Flash memory	19.1	13.2	mA
I_{DD}	SLEEP	Internal clock source	48M	Flash memory	15.4	9.3	mA
I_{DD}	DEEP SLEEP	Internal clock source	48M	Flash memory	14.7	8	mA

1. Guaranteed by design, not tested in production.

Typical current consumption in Stop state of low power mode

Symbol	Parameter	Condition	Typical Value	Unit
I_{DD}	Stop	LSI on, LPTIM enabled	6.1	uA
		LSI off	3.8	

1. Guaranteed by design, not tested in production.

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Wake-up time from low power mode

The wake-up times listed in the table below are measured during the internal clock wake-up phase. The clock source used for wake-up depends on the current operating mode:

(1) SLEEP or DEEP SLEEP mode: The clock source is determined by the actual setting.

(2) STOP mode: The clock source is LSI.

Symbol	Parameter	Condition	Typical Value	Unit
T_{LPIDLE}	Wake up from SLEEP mode	The clock used is HSI	20	ns
$T_{LPSLEEP}$	Wake up from DEEP SLEEP mode	The clock used is HSI	200	ns
T_{LPSTOP}	Wake up from STOP mode	Use LPTIM as the wake-up source	15 25	us us

1. Guaranteed by design, not tested in production.

4.2.5 Internal Clock Source Characteristics

The characteristic parameters given in the table below are measured under conditions where the ambient temperature and supply voltage comply with the general operating conditions.

High-speed internal (HSI) oscillator

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit
f_{HSI}	Frequency	V_{DD}=5V		48		MHz
ACC_{HSI}	HSI clock accuracy	V_{DD}=5V, TA = -40°C~ 105°C	-2.5		+2.5	%
		V_{DD}=5V, TA = 25°C	-1		+1	%

Note: The above results are measured at VDD = 5V. The chip is factory-calibrated with HSI values for VDD ranging from 2.2V to 5V. When the chip operates at non-5V VDD, it is recommended to call the HSI calibration function in the firmware library to adjust the HSI calibration value for higher HSI clock accuracy.

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

Low-speed internal (LSI) oscillator

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit
f_{LSI}	Frequency	V_{DD}=5V		32.768		KHz
ACC_{LSI}	LSI clock accuracy	V_{DD}=2.5~5V, TA = -40°C~105°C	-5		+5	%
		V_{DD}=5V, TA = 25°C	-1		+1	%
$Tstab_{(LSI)}$	LSI startup time (maximum configuration)	V_{DD}=5V, TA = 25°C		260		us
$IDD_{(LSI)}$	LSI power consumption	V_{DD}=5V, TA = 25°C		2.3		uA

4.2.6 Storage Characteristics

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit
t_{prog}	Byte programming time		-	6	6.5	us
t_{ERASE}	Page (512 bytes) erase time		-	2.6	3	ms
t_{ME}	Full chip erase time		-	35	40	ms
I_{DD}	Supply current	Read current	-	3.5	5.5	mA
		Programmable current	-	-	2	mA
		Erasing current	-	-	1.5	mA
N_{END}	Erasing times		100,000	-	-	Cycles
T_{DR}	Data retention period	TA = 85°C	20	-	-	Years
		TA = 25°C	100	-	-	Years

1. Guaranteed by design, not tested in production.

4.2.7 I/O Port Characteristics

General I/O characteristics

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

V_{IL}	Input low-level voltage	V_{DD}=5V			1.5	V
V_{IH}	Input high-level voltage	V_{DD}=5V	3.5			V
R_{PU}	Pull-up equivalent resistance	V_{IN}=V_{SS}		40		kΩ
R_{PD}	Pull-down equivalent resistance	V_{IN}=V_{DD}		40		kΩ
C_{IO}	I/O pin capacitance				11	pF

1. Guaranteed by design, not tested in production.

Output drive current

The GPIO ports can sink or output up to ±20mA of current.

In user applications, the number of I/O pins must ensure that the drive current does not exceed the given absolute maximum rating:

(1) The total current drawn from V_{DD} by all I/O ports, plus the maximum operating current of the MCU from V_{DD}, must not exceed the absolute maximum rating I_{VDD}.

(2) The total current sunk by all I/O ports and flowing out through V_{SS}, plus the maximum operating current of the MCU from V_{SS}, must not exceed the absolute maximum rating I_{VSS}.

4.2.8 NRST Pin Characteristics

Unless otherwise noted, the parameters listed in the table below are measured under conditions where the ambient temperature and V_{DD} supply voltage comply with the specified conditions.

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!
Developer Microelectronics Confidential

$V_{IL(NRST)}$	NRST input low-level voltage	V_{DD}=5V			1.5	V
$V_{IH(NRST)}$	NRST input high-level voltage	V_{DD}=5V	3.5			V
R_{PU}	Pull-up equivalent resistance	V_{IN} = V_{SS}		40		kΩ
$V_{F(NRST)}$	Input low-level duration		23			us

1. Guaranteed by design, not tested in production.

4.2.9 ADC Characteristics

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit
V_{ADCIN}	Input voltage		V_{SS}		V_{DD}	V
F_{ADCCLK}	ADC work clock				16	MHz
$T_{ADCSTART}$	ADC startup time				1	us
$T_{ADCCONV}$	Conversion time (including sampling time)	f_{ADC_CLK}=16MHz, $T_{ADCCONV}$=2 ADC_CLK sampling + 14 ADC conversion time		1		us
ENOB	Effective Bits	1Msps@REF=VDD		10.3		Bit
SNR	Signal to Noise Ratio	1Msps@REF=VDD		66		db
DNL	Differential nonlinear error				0.6	LSB
INL	Integral nonlinear error				2	LSB
E_o	Offset error			21		mV

1. Guaranteed by design, not tested in production.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

4.2.10 I2C Characteristics

Symbol	Parameter	Standard Mode (100°K)		Fast Mode (400°K)		High-speed Mode (1M)		Unit
		Min Value	Max Value	Min Value	Max Value	Min Value	Max Value	
t_{SCLL}	SCL clock low time	4.7		1.3		0.5		us
t_{SCLH}	SCL clock high time	4.0		0.6		0.26		us
$t_{SU.SDA}$	SDA setup time	250		100		50		ns
$t_{HD.SDA}$	SDA hold time	0		0		0		ns
$t_{HD.STA}$	Start condition hold time	4.0		0.6		0.26		us
$t_{SU.STA}$	Repeated start condition setup time	4.7		0.6		0.26		us
$t_{SU.STO}$	Stop condition setup time	4.0		0.6		0.26		us
t_{BUF}	Bus idle (stop condition to start condition)	4.7		1.3		0.5		us

1. Guaranteed by design, not tested in production.

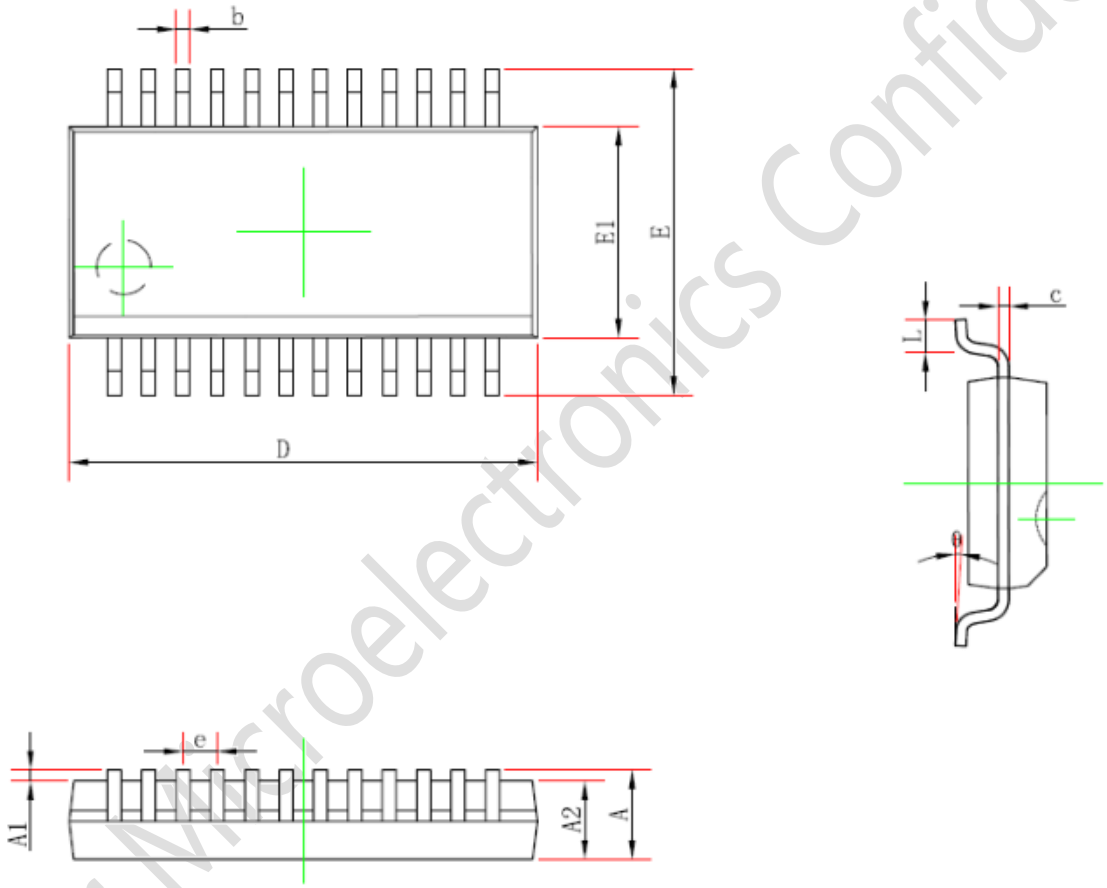
Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

5 Package Information

5.1 SSOP24 Package Information

- SSOP24 plastic package specification diagram



	mm	
	Min	Max
A	—	1.95
A1	0.05	0.35
A2	1.05	—
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	

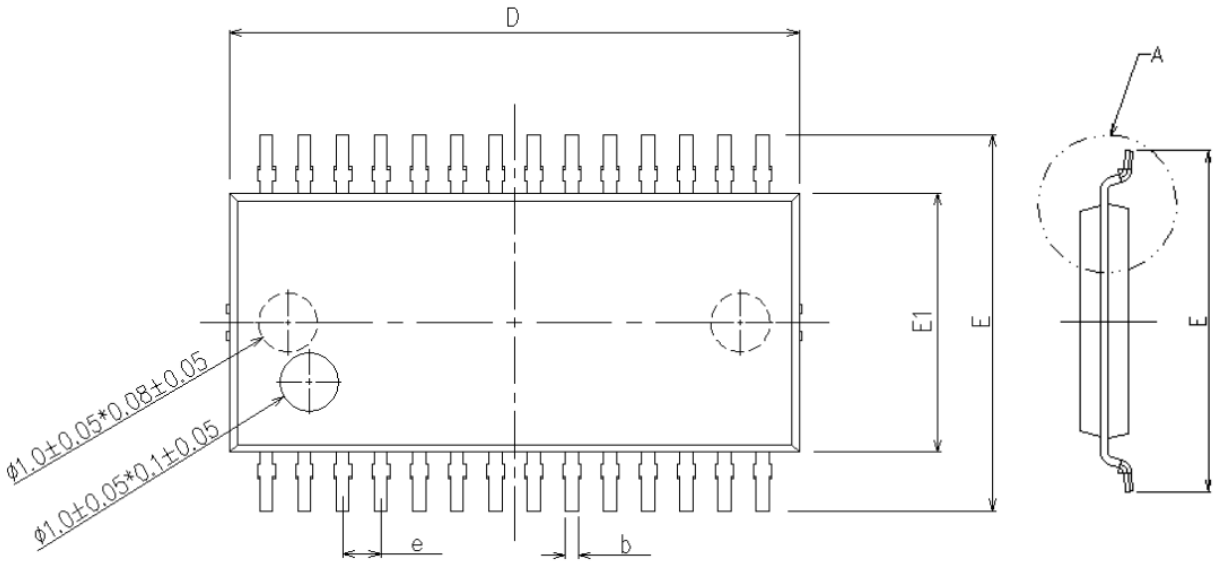
Developer Microelectronics Confidential

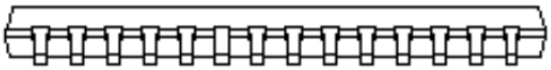
The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

L	0.3	1.5
θ	0°	10°

5.2 TSSOP28 Package Information

- TSSOP28 plastic package specification diagram



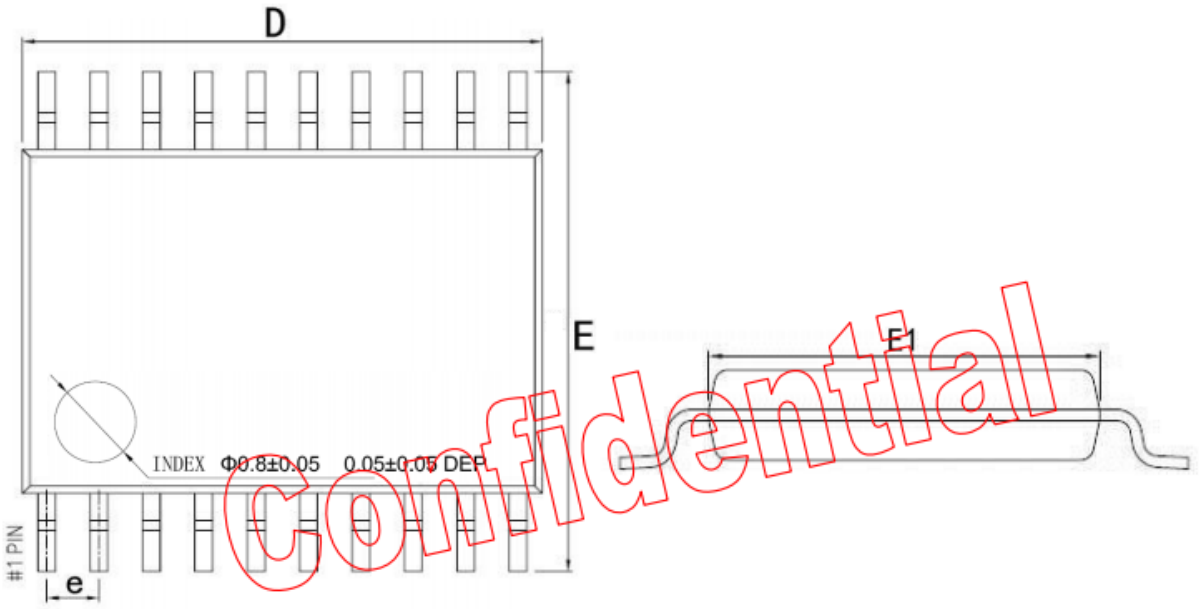


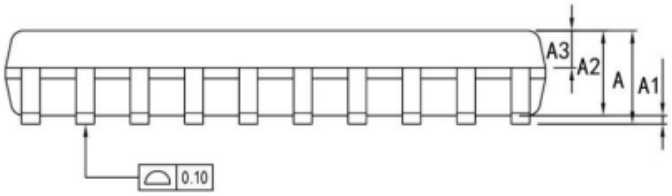
	mm		
	Min	Nom	Max
A	1.05	1.10	1.15
A1	0.05	0.10	0.15
A2	0.90	1.000	1.05
b	0.195	0.220	0.245
c	0.119	0.127	0.135
c1	0.139	0.147	0.155
D	9.6	9.7	9.8
E		6.4 BSC	
E1	4.300	4.400	4.500
e	0.625	0.650	0.675
L	0.45	0.690	0.75
L1		1.00 REF	
L2		0.254	
Θ	0°	—	8°

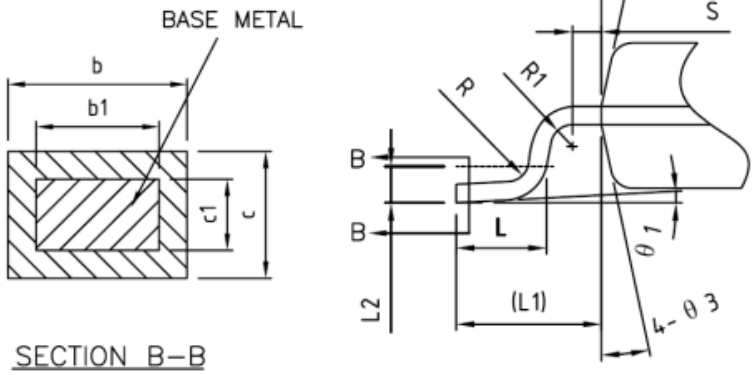
The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

5.3 TSSOP20 Package Information

- TSSOP20 plastic package specification diagram







名称	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
D1	4.00	4.20	4.40
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e	–	0.65BSC	–
L	0.45	0.60	0.75
L1	–	1.00REF	–
L2	–	0.25BSC	–
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

	mm		
	Min	Nom	Max

Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

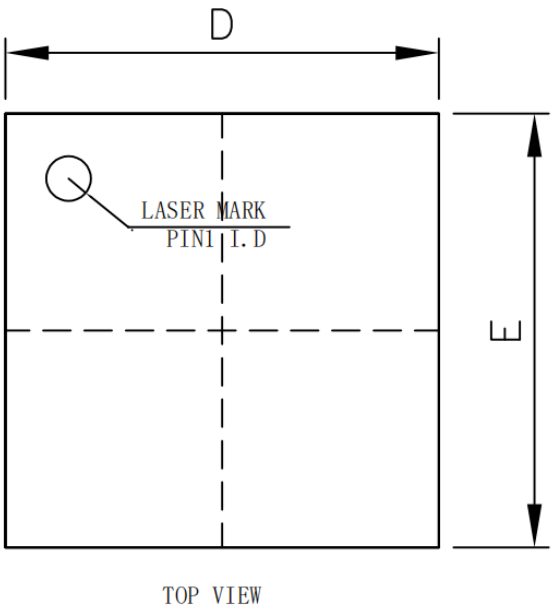
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
b	0.20	—	0.28
b1	0.20	0.22	0.24
c	0.10	—	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
D1	4.00	4.20	4.40
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e	—	0.65BSC	—
L	0.45	0.60	0.75
L1	—	1.00 REF	—
L2	—	0.25BSC	—
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
θ1	0°	—	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

Developer Microelectronics Confidential

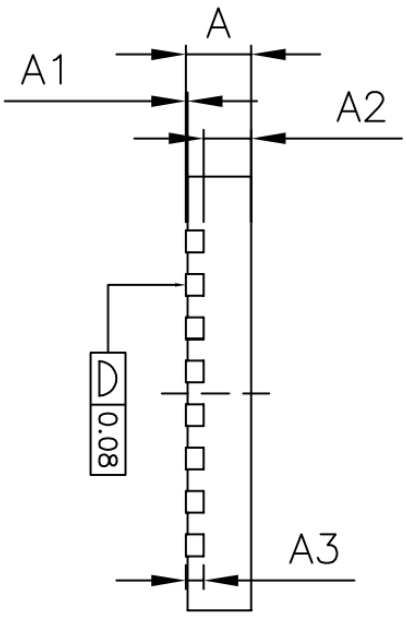
The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

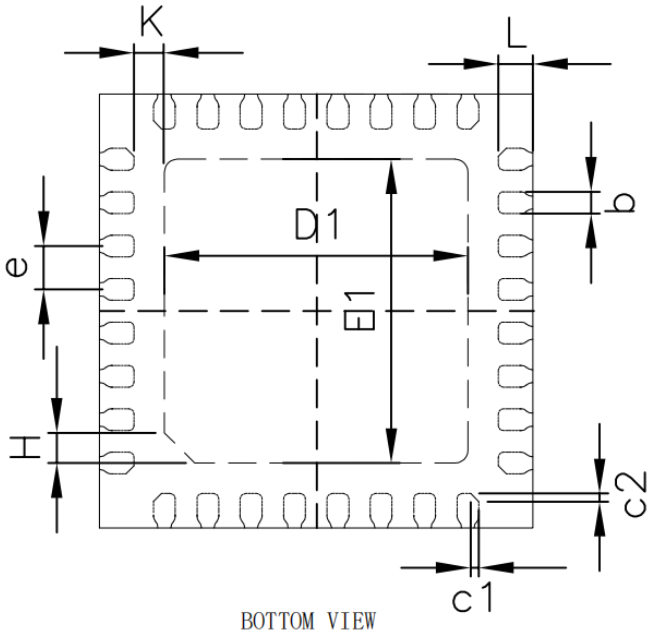
5.4 QFN32 Package Information

- QFN32 plastic package specification diagram



TOP VIEW





BOTTOM VIEW

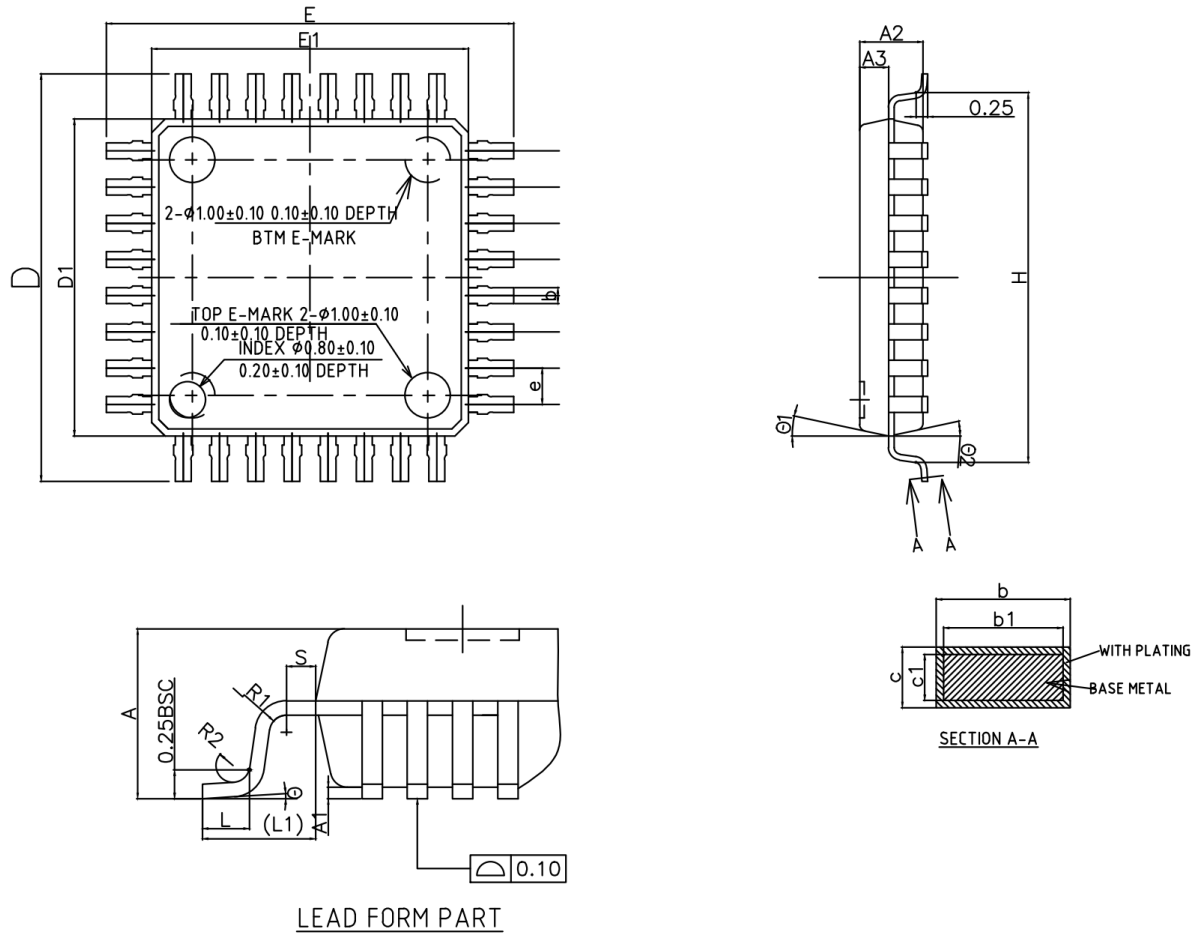
	mm		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.479	0.547	0.597

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

A3	0.203REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D1	3.40	3.50	3.60
E1	3.40	3.50	3.60
e	0.5BSC		
K	0.35REF		
L	0.350	0.400	0.450
H	0.35REF		

5.5 LQFP32 Package Information

- LQFP32 plastic package specification diagram



	mm		
	Min	Nom	Max
A	—	—	1.60

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	0.35	0.42
b1	0.32	0.35	0.42
c	0.13	—	0.18
c1	0.120	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.8BSC		
H	8.14	8.17	8.20
L	0.50	0.6	0.70
L1	1.00REF		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

6 Revision History

Revision History

Ver.	Revision Date	Revision Content
V0.8	2023.11.13	Initial version
V0.9	2024.01.08	Updated ADC channel description and package information, etc.
V1.0	2024.01.23	Updated the section on storage mapping
V1.1	2024.07.05	1. Updated the number of 32-bit TIMs to 3 2. Updated TSSOP24 to SSOP24 on the pinout diagram

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

7 Declarations

Developer Microelectronics makes every effort to ensure the accuracy and reliability of the content in this product specification, but reserves the right to modify the content of the specification without further notice. Customers should contact Developer Microelectronics to obtain the latest relevant information and verify that the information is complete and up-to-date before placing an order. All product sales are governed by the company's terms and conditions of sale provided at the time of order confirmation.

Developer Microelectronics periodically updates the content of this document, and actual product parameters may vary depending on the model or other factors. This document does not constitute any express or implied warranty or authorization.

This product specification does not contain any license for intellectual property rights owned by Developer Microelectronics or any third party. Developer Microelectronics makes no express or implied warranty regarding the information contained in this product specification, including but not limited to the accuracy of the specification content, merchantability, fitness for a particular purpose, or non-infringement of the intellectual property rights of Developer Microelectronics or any third party. Developer Microelectronics is not liable for any incidental or consequential loss related to this specification or its use.

Developer Microelectronics assumes no obligation for application assistance or customer product design. Customers are solely responsible for their use of the company's products and applications. To minimize risks associated with customer products and applications, customers should provide adequate design and operational safety validation.

Without authorization from Developer Microelectronics, no third party is permitted to use, copy, or convert the contents disclosed in this specification. If any unauthorized use is found, the company will pursue legal action and seek compensation for any losses incurred.

Please ensure that products are used within the conditions specified in this document, paying particular attention to absolute maximum ratings, operating voltage ranges, and electrical characteristics. Developer Microelectronics assumes no responsibility for any damage resulting from the use of products outside the conditions specified in this document, including any faults and/or accidents.

Developer Microelectronics is committed to improving product quality and reliability, but all semiconductor products have a certain failure rate, which may lead to incidents such as personal injury or fire. When designing products, please carefully consider redundant designs and safety margins to avoid accidents.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!

When using the company's ICs in products, the company assumes no responsibility for any patent disputes that may arise due to the methods of using the IC in the product, the product specifications, or due to reasons related to the country of importation, including any disputes involving products that contain this IC.

Developer Microelectronics Confidential

The contents of this document are confidential. No organization or individual is permitted to reproduce or distribute it in any form without authorization!