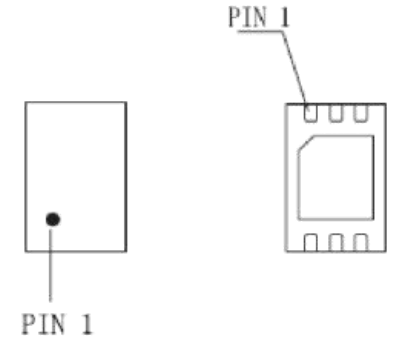
## GENERAL DESCRIPTION

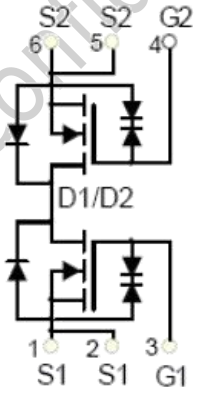
The DP8203 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge.
It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

## PRODUCT SUMMARY

| | |
|---|---|
| $V_{DS}$ | 16V |
| $I_D$ (at $V_{GS}$=4.5V) | 10.0A |
| $R_{DS(ON)}$ (at $V_{GS}$ = 4.5V) | < 7.5mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ = 4.0V) | < 8.0mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ = 3.7V) | < 8.5mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ = 3.1V) | <9.0mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ = 2.5V) | < 9.5mΩ |

**ESD Protected**




## ABSOLUTE MAXIMUM RATINGS (TA=25°C unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 16 | V |
| Gate-Source Voltage | $V_{GS}$ | ±10 | V |
| Continuous Drain Current | $I_D$ | 10 | A |
| Pulsed Drain Current | $I_{DM}$ | 50 | A |
| Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 150 | ℃ |

## THERMAL CHARACTERISTIC

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Maximum Junction-to-Ambient | Steady-State | $R_{\theta JA}$ | 83.3 | ℃/W |

# ELECTRICAL CHARACTERISTICS (TA=25℃ unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typc | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V,$I_D$=250μA | 16 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=16V,$V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±4.5V,$V_{DS}$=0V | - | - | ±1 | μA |
| | | $V_{GS}$=±10.0V,$V_{DS}$=0V | - | - | ±10 | μA |
| **On Characteristics** [a] | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 0.5 | 0.7 | 1.0 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=4.5V, $I_D$=3.0A | 5.0 | 6.0 | 7.5 | mΩ |
| | | $V_{GS}$=4.0V, $I_D$=3.0A | 5.3 | 6.3 | 8.0 | mΩ |
| | | $V_{GS}$=3.7V, $I_D$=3.0A | 5.5 | 6.5 | 8.5 | mΩ |
| | | $V_{GS}$=3.1V, $I_D$=3.0A | 6.0 | 7.5 | 9.0 | mΩ |
| | | $V_{GS}$=2.5V, $I_D$=3.0A | 6.5 | 8.0 | 9.5 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=5V,$I_D$=7A | 9 | 36 | - | S |
| **Dynamic Characteristics** [b] | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=10V, $V_{GS}$=0V, F=1.0MHz | - | 2150 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 350 | - | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 260 | - | pF |
| **Switching Characteristics** [b] | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=10V, $R_L$=1.35Ω $V_{GS}$=5.0V, $R_{GEN}$=3Ω , | - | 2.5 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 6.7 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 43 | - | nS |
| Turn-Off Fall Time | $t_f$ | | - | 11 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=10V, $I_D$=7A, $V_{GS}$=4.5V | - | 19 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 2.2 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 5.3 | - | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage | $V_{SD}$ | $V_{GS}$=0V,$I_S$=1.0A | - | - | 1.0 | V |
| Diode Forward Current [a] | $I_S$ | - | - | - | 6.0 | A |



Notes

a.Pulse Test:Pulse Width ≤ 300us, Duty Cycle ≤ 0.5%.

b.Guaranteed by design, not subject to production testing.

# TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

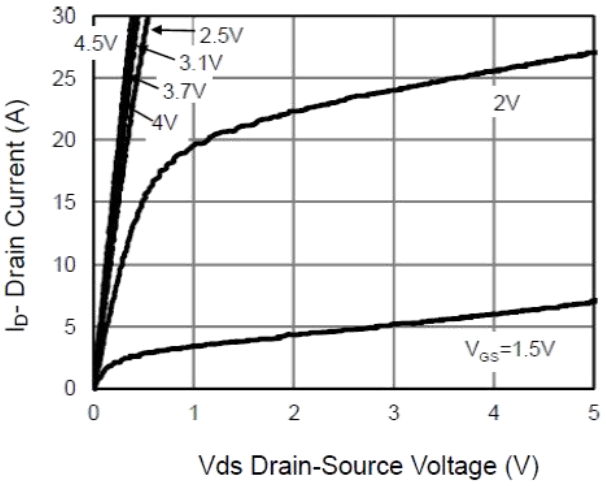



**Figure 1 Output Characteristics**

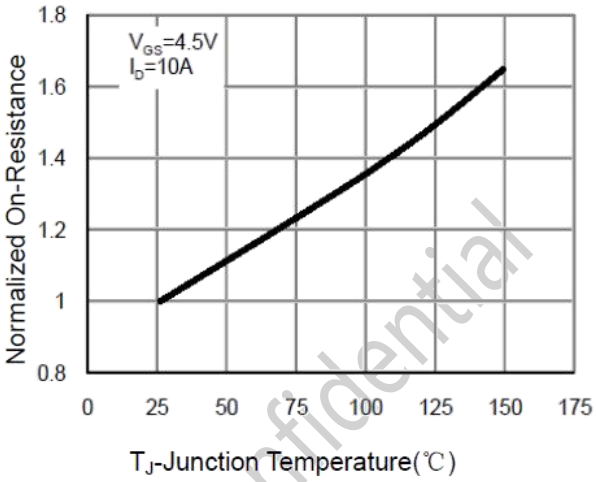



**Figure 4 Rdson-Junction Temperature**

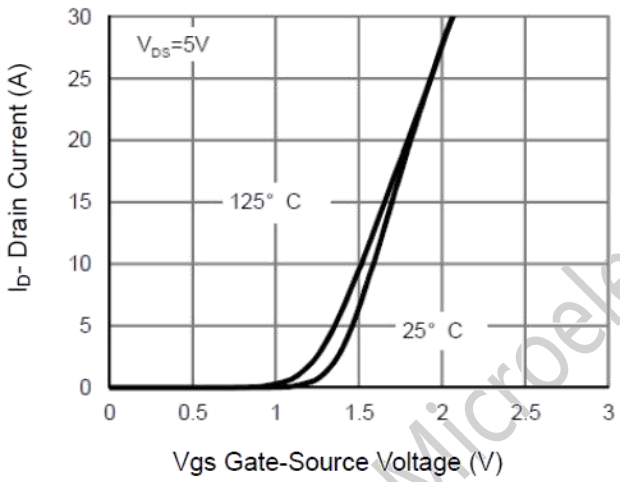



**Figure 2 Transfer Characteristics**

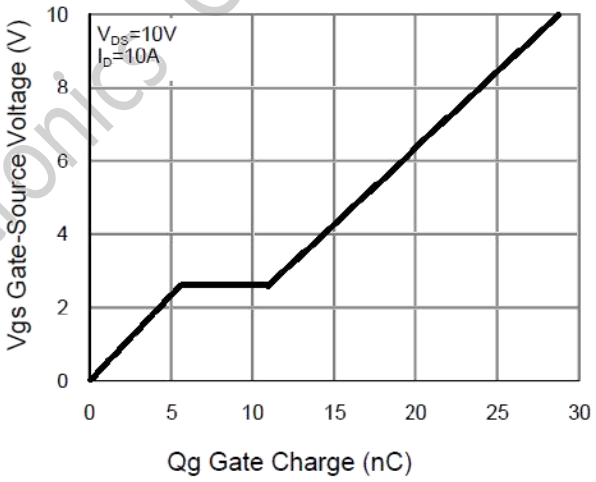



**Figure 5 Gate Charge**

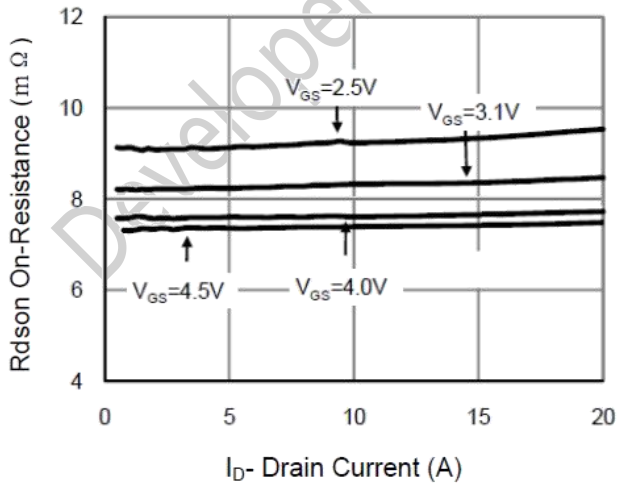



**Figure 3 Rdson- Drain Current**

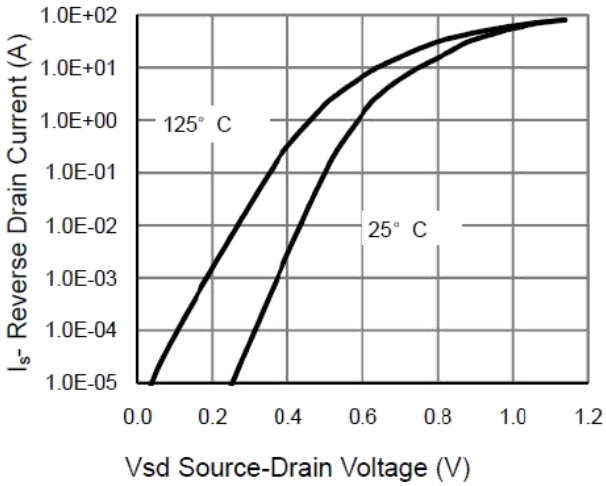



**Figure 6 Source- Drain Diode Forward**

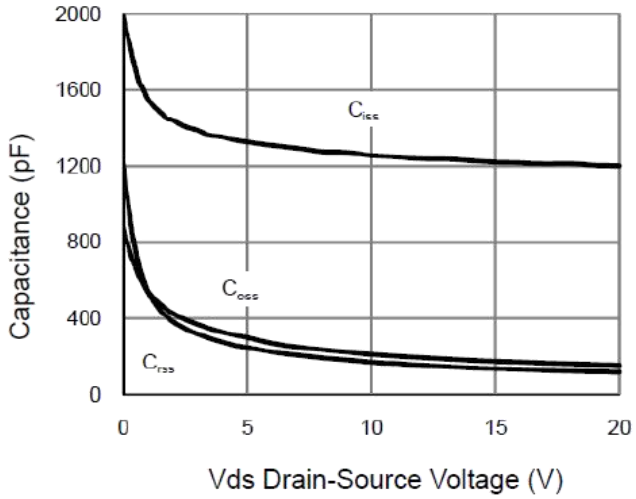



**Figure 7 Capacitance vs Vds**

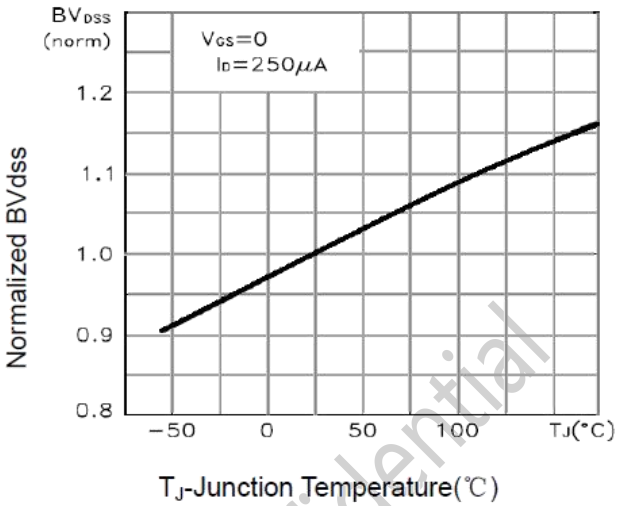



**Figure 9 $BV_{DSS}$ vs Junction Temperature**

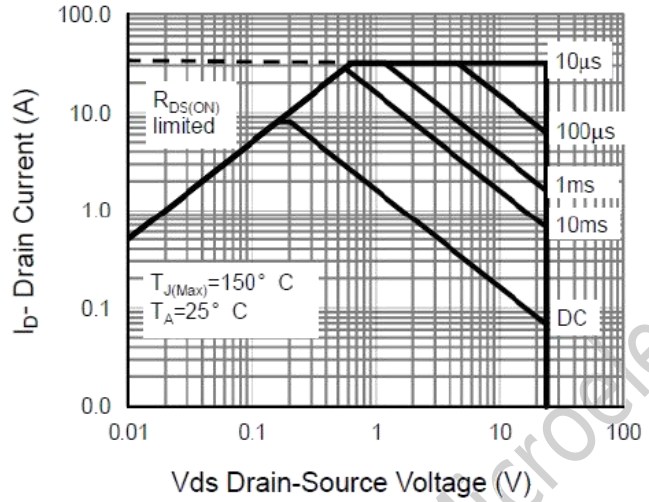



**Figure 8 Safe Operation Area**

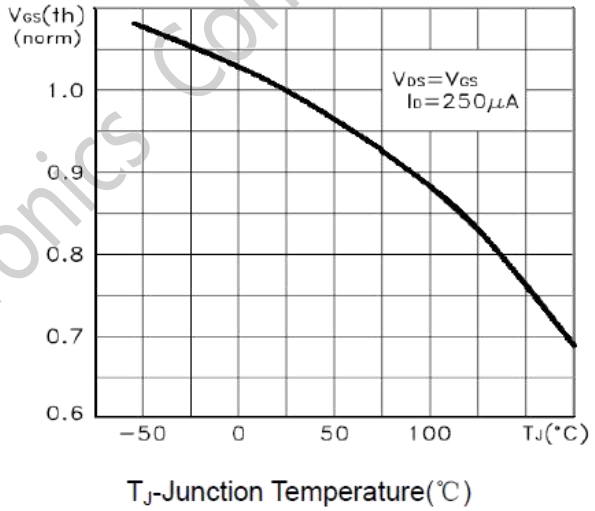



**Figure 10 $V_{GS(th)}$ vs Junction Temperature**

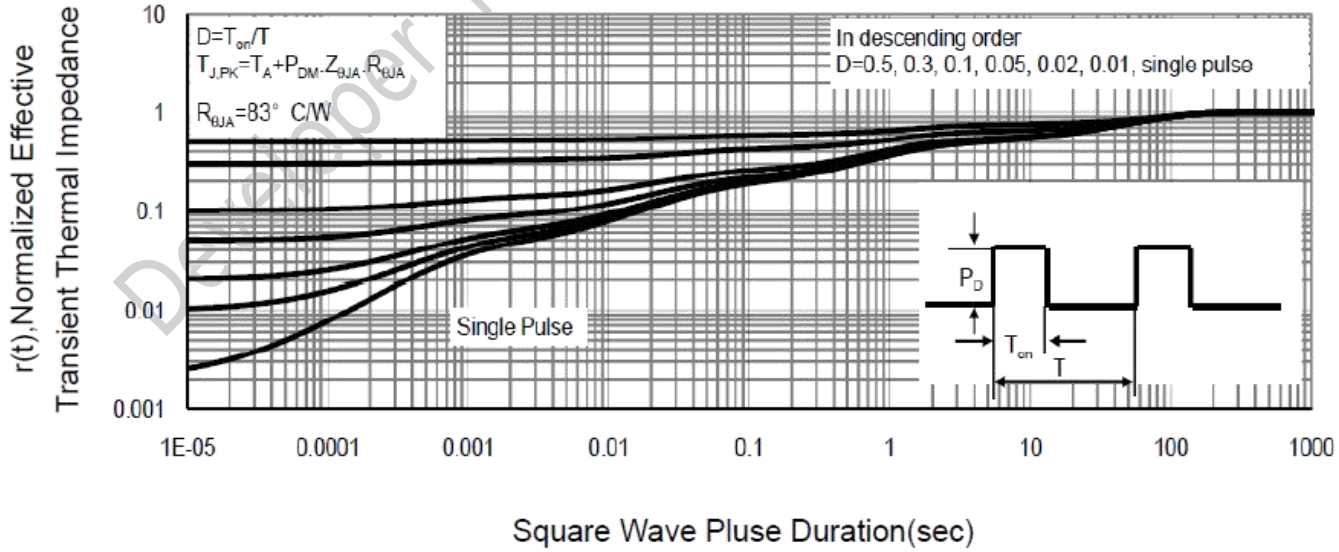
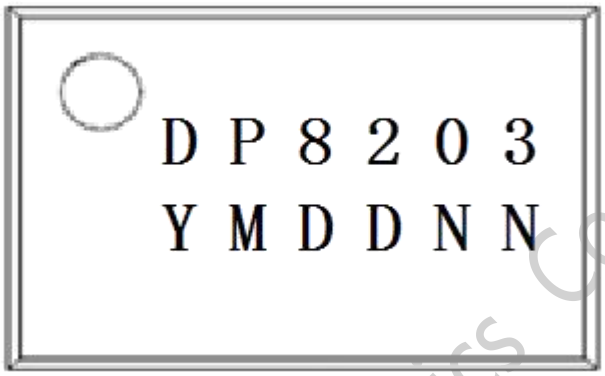



**Figure 11 Normalized Maximum Transient Thermal Impedance**

# MARKING DESCRIPSION

**TDFN2X3-6L**




**NOTE:**

Y —Code of productive year code(the last number of the year)

M —Code of productive month(for example: A means January, B means February…)

DD —Productive date(the number of the date)

NN —Lot number of wafer

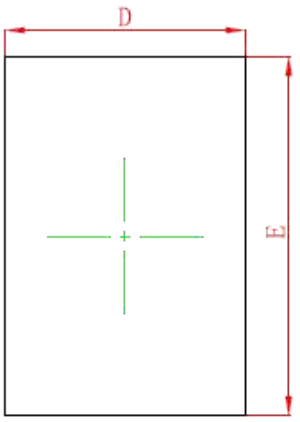
**FOR EXCAMPLE:**

5G1103

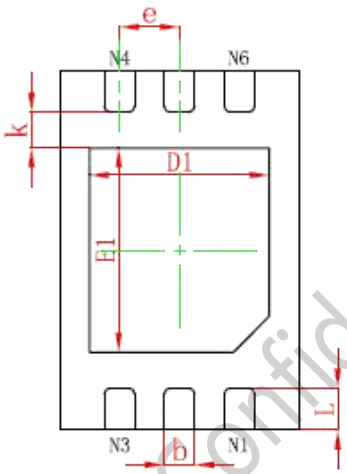
Means this product was produced in 2015-07-11 , and 03 is the wafer lot.

# PACKAGE OUTLINE DIMENSIONS

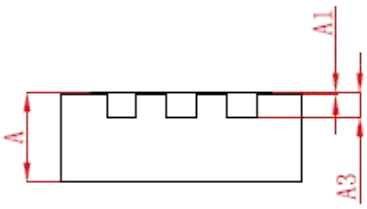
**TDFN2X3-6L**




TOP VIEW



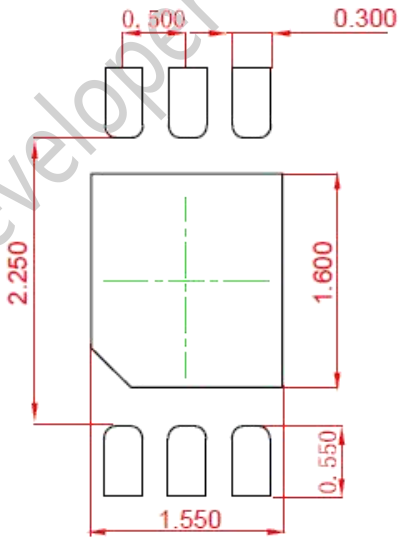

BOTTOM VIEW




SIDE VIEW

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.203REF. | | 0.008REF. | |
| D | 1.950 | 2.050 | 0.077 | 0.081 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| D1 | 1.450 | 1.550 | 0.057 | 0.061 |
| E1 | 1.650 | 1.750 | 0.065 | 0.069 |
| k | 0.200MIN. | | 0.008MIN. | |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| e | 0.500TYP. | | 0.020TYP. | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

# SUGGESTED PAD LAYOUT




Note:
1.Controlling dimension:In millimeters.
2,General tolerance:±0.050mm.
3.The pad layout is for reference purposes only.

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